A Tricolor-Pixel Digital-Micromirror Video Chip

by

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Committee in charge:

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Abstract

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This dissertation describes a new method for reproducing color still or moving images using microelectromechanical system (MEMS) technology to create a light valve fabricated from surface-micromachined polycrystalline silicon (poly). A light valve modulates light from a conventional source that is directed onto it and passes or reflects part of the light into a viewing system, which is usually a projection lens.

Light valves have a long history of innovation going back to 1940. In the 1980s and 1990s, researchers at Texas Instruments, Inc. developed a type of light valve that operates digitally. Each of its picture elements (pixels) is a single micromechanical mirror fabricated on top of a standard CMOS memory cell. Each mirror is suspended by a torsion spring that allows the mirror to tilt into two positions. In the “on” position, light is reflected into the projection lens to become part of the image, while in the “off” position,

the light is reflected away from the projection lens and into a light-absorbing sink. These two positions are used in a pulse-width modulation scheme to achieve variable intensities. Color images have been assembled using multiple light valves, by time-division multiplexing primary colors from the light source, or by a combination of these techniques.

The novel method for generating color images described here employs three mirrors to form each pixel, one for each primary color. Light that has been separated into primary colors is directed onto the light valve from three directions. The tilt axis of each mirror is perpendicular to the path of that mirror's illumination. When a mirror tilts into the "on" position, it reflects light of only the corresponding color into the projection lens; the light from the other two sources is reflected into light sinks. The resulting image is spatially color-multiplexed as in a color CRT or LCD image. The image does not require convergence and avoids image artifacts due to time-division multiplexing.

By fabricating this light valve from poly instead of aluminum, we can avoid fatigue and deformation problems and can eliminate the need to build on top of CMOS circuitry.

Demonstration devices utilizing five levels of poly and ten mask steps have been successfully fabricated and tested in the Berkeley Microfabrication Laboratory. In addition, a new tight-tolerance hinge design and a design method allowing for post-release metallization have been implemented in Sandia National Laboratory's four-level poly, 11-mask SUMMiT process.

This work was funded by the Berkeley Sensor & Actuator Center (BSAC).

Approved by: _____

Committee Chair

Dedication

I dedicate this work to my family — my parents, George and Nancy, and the many long nights at the dining room table — My loving wife, Linda, without whose encouragement and assistance I would surely have abandoned this enterprise — and my children, Heather, Gretchen and Frederick, who inspire me and give me great hope for the future.

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Preface

Displays have been a passion of mine since I was an undergraduate. My first attempt at a masters degree project was turning a television into a dumb terminal. My involvement increased when I needed a display for a briefcase computer and found a single line vacuum-fluorescent tube to incorporate. Engineers who saw the briefcase computer didn't care much for the computer, but they wanted to buy the display. And so began an odyssey of dozens of displays and touch panel systems. When I saw an article in IEEE Spectrum magazine in December of 1993 on digital micromirror displays, I was immediately hooked. I just had to work on improvements that popped into my head, so I became a student researcher in the Berkeley Sensor & Actuator Center (BSAC).

Most of the improvements that I envisioned have since been incorporated by Texas Instruments, Inc. Some of the improvements were in progress at the time the article was published, even though they weren't included. But the major vision that I had was to bring a new way of generating color images to this technology.

It was my vision then that this technology would make major inroads against the cathode-ray tube, and that eventually, most televisions, desktop computer monitors and visor-mounted displays would be based on digital micromirrors. Since that time, liquid-crystal displays have made major inroads into the computer monitor market, and micromirrors are still too expensive to compete in that market. Since we now have three-pound micromirror projector systems and large-screen rear-projection televisions, it seems we only need to wait for the costs to fall far enough to be competitive in the desktop market.

Many of the figures in this thesis are colored in the original. The copy which is filed in the university library is in color. Additionally, this work is available in Adobe Acrobat portable document format that, when viewed on a color display, will render the colors and higher resolution images. An attempt was made to make these figures intelligible in black by using various line and fill patterns.

Acknowledgments

I would like to thank:

Professor Richard White for being my advisor and treating me as a colleague and for being a friend, for allowing me to help develop course materials and to co-author a textbook with him;

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And both Texas Instruments, Inc.[1] and Sandia National Laboratories for graciously letting me use their copyrighted materials in this thesis.

1. Digital Light Processing, DLP, Digital Micromirror Device and DMD are trademarks of Texas Instruments.

1. Background

The subject of this dissertation is a micro-electromechanical system (MEMS) to be used for forming optical images. The device is fabricated using surface micro-machining techniques[1], on a silicon wafer like those used in making integrated circuits. A fully functional device would consist of several hundred-thousand microscopic mirrors (the research chip has over eighteen thousand) that tilt to redirect light. The micromirror chip can reproduce or synthesize moving or still optical color images (video or computer images) from digital data.

To be used, the chip needs to be incorporated into a projector very much like a 35mm slide projector. The chip replaces the slide, and the light shines on the front of the chip from a position 20° away from the normal (instead of from the back, as in a slide projector). Unlike a static slide, the chip can generate any image for which we supply the digital data.

1.1 Previous Efforts

The desire to present audiences with large moving images has driven many technological efforts since the 1830s. First came gadgets that sequentially displayed drawings, then photography made it possible to show more accurate images. These led to the invention of the movie camera in 1887 by Thomas Alva Edison, and the movie projector in 1895 by Auguste and Louis Lumiere. By 1907, the cathode-ray tube (CRT) had advanced far enough to allow Boris Rosing to patent a television system using it. One of his students, Vladimir Zworykin, working at Westinghouse, developed the first practical television CRT in 1929[2], and, in 1933, while at RCA, developed an electronic camera tube to complete the all-electronic television. Broadcasts started in London in 1936, and after the National Television Standards Committee (NTSC) standard was developed, in the United States in 1941.

The effort to move television from the small screen to the large theater screen began in the early 1940s with three different approaches. First, RCA introduced a CRT with Schmidt optics, which operates much like a Schmidt telescope in reverse with the CRT replacing the eyepiece, and a large spherical mirror gathering the light and reflecting it through a correction lens onto the screen. Next came the Eidophor, which bounces light, produced by an arc, off a thin oil film on the inside of a rotating reflective bowl. The desired image is created by a raster-scanned electron beam that causes the oil to diffract the light, sending it around a light stop and into the projection lens. This was the first instance of a light-valve technology where the light source is separate from the modulation mechanism. The third approach was the Scophony[3], a device that was in some ways similar to modern laser printers. Light from an arc-lamp was passed through an acousto-optic modulator filled with liquid and driven by a quartz crystal. The image information propagated down the length of the device, which corresponded to the width of the image. A synchronous rotating polygonal mirror convolved the image of the moving wavefront to a stationary position on the screen during its trip down the tube. This meant that an entire line of the image was illuminated on the screen, rather than just a point as with a CRT. Vertical deflection was provided by a second moving mirror. Scophony modulation is still used today in high-power laser projectors[4].

In 1972, the Advent Corporation brought out a three-CRT, three-lens projection television system[5]. Each CRT produced a single color image — red, blue or green — and the images were combined on the screen. Convergence was challenging and had to be re-done if the projector or screen was moved. The convergence problems were greatly reduced in later models by using special dichroic mirror-prisms to combine the light before projecting with a single lens. This prism technique is used in modern liquid-crystal display (LCD) projectors, and a variant is used with multi-chip micromirror systems such as those discussed below.

Hughes Research Laboratories announced a photoactivated liquid-crystal light valve (LCLV) system in 1973[6]. This device amplified the image it received on one side (typically from a CRT), modulating the bright light reflecting off of the other side. Inherently analog in nature, it had no discrete pixels; instead it relied on the assumed linear behavior of the liquid-crystal material, and it required three devices to project full-color images. Successors of this device are commonly used to project large video images in theaters.

Micromechanical light-valve systems entered the scene in 1968 when K.P. Preston of Perkin-Elmer created a membrane light modulator for use in optical computing[7]. Preston used a metallized film that was supported by a grid that divided it into pixels. Each pixel was deformed using electrostatic force produced across an air-gap by an electrode located under it.

In 1970, J.A. van Raalte of RCA Laboratories disclosed a deformable metal membrane array[8]. Packaged in a vacuum tube, each pixel was a thin metal alloy that was supported off of the glass faceplate by an aluminum grid. An electron beam was used, as in a CRT, to deposit charges on the glass faceplate through a hole in the center of each pixel. The charge caused the metal membrane to deform toward the glass. Light reflected from the pixels through the glass faceplate hit a stop when the pixel was flat, but when the membrane was deformed, the light missed the stop and entered into the projection lens. The greater the deflection the more light would make it past the stop.

A combination of Preston's and van Raalte's techniques, reported in 1990[9][10], used the electron beam to address a charge-transfer plate behind each pixel. The metallized film was deformed toward the plate to steer light around a stop.

Another approach, the Mirror Matrix Tube, was developed at Westinghouse in 1973 by Guldberg and Nathanson[11]-[14]. This was a silicon-on-sapphire structure that used an electron beam to address the individual pixels. Fabricated with a single photo-

lithographic step, this clever design patterned the pixel shape into an oxide layer grown on the silicon and then used a wet etch to remove the underlying silicon except for a post in the center of each pixel. The entire structure was then aluminized, the transparent pixels became mirrors, and the aluminum that fell between the pixels formed a grid toward which the edges of the pixels were electrostatically deflected. To better allow the pixels to deflect, a slot was patterned into each side of the pixel, resulting in the shape shown in Figure 1.1. After the microfabrication, the sapphire substrate was bonded to a vacuum-

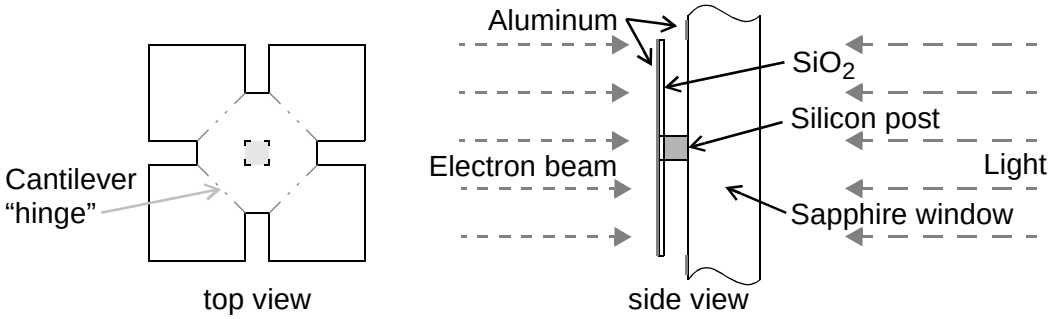


Figure 1.1 Mirror Matrix Tube pixel

tube structure much like a CRT. This device, like the others that came before it, was analog in nature — as a pixel deflects more it sends more light into the projection lens around a light stop. IBM later disclosed a method for making each wing a separate pixel, thereby increasing the resolution[15].

These devices that deform tiny mirrors came to be known collectively as deformable mirror devices, or DMDs, an acronym that would later be given a new meaning.

Texas Instruments, Inc. (TI) worked on other analog deformable mirror devices from 1977 to 1987. These were designed to be microfabricated on top of a charge-coupled device (CCD), a technology typically used to make integrated circuit imaging arrays. The early devices operated very much like the membrane light modulator, except for the drive electronics. In 1980, several silicon micromachined cantilever mirror designs were tried but abandoned because the high-temperature steps required were incompatible with the

aluminum wiring on the underlying circuit. A low-temperature process that employed aluminum mirrors and photoresist as a sacrificial layer was developed in 1983, but all of these, like their predecessors, were analog in operation, and suffered from low contrast ratios (the ratio of intensities of full-on to full-off light).

In late 1987, TI came up with the revolutionary *Digital Micromirror Device*™ light valve (which they also called a DMD, a term they later trademarked — a move considered controversial by some). The structure and operation of this device will be explained in greater detail in Section 1.2.

Aura Systems, Inc. patented a piezoelectric-mirror analog light valve in 1993. This device used a pair of piezoelectric devices with opposite polarity voltages applied to tilt a micromirror up to ±0.25°.

The material in this Section (1.1) is drawn mostly from an excellent article by Larry Hornbeck[16], inventor of the TI Digital Micromirror Device™ chip. He, however, ignores a great deal of development that went on in this field at IBM. Kurt Peterson and others there made many discoveries that are documented in the *IBM Technical Disclosure Bulletin* as early as 1977[17]-[27] and in patents[28]-[33]. Other patents that Hornbeck ignores include one by Kodak, filed in 1974, for a “hinged” mirror structure[34], one by Henry Guckel filed in 1978[35], and others by RCA[36][37].

1.2 Basic Operating Principles of the TI Digital Micromirror Device™ Chip

A DMD™-chip-based projector is very much like a slide or movie projector in that a projection lens focuses an image of the chip onto the screen.

In a film-based projector, the light comes from behind the slide and is “filtered” by the film. Light that passes through the film and into the lens ends up on the screen, as shown in Figure 1.2. Any light that is reflected or scattered outside the lens by the film, or by dust or scratches on the film, is lost.

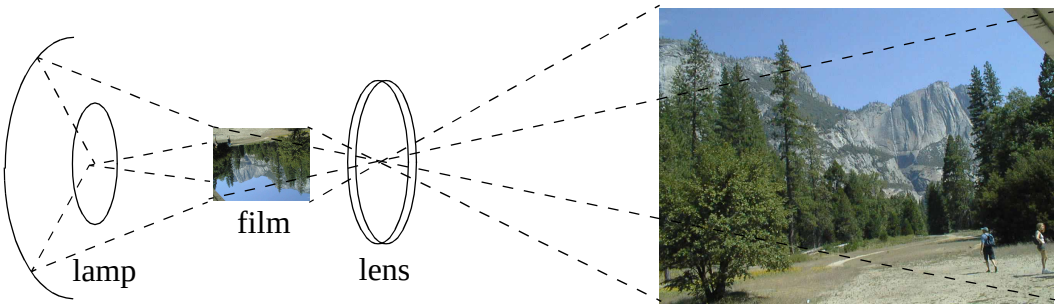


Figure 1.2 Film projector optics

In the DMD™ projector, the light comes from a source in front of the DMD™ chip, but at an angle of about 20° from the normal to the DMD™ chip, as shown in Figure 1.3. The image is formed by the array of mirrors on the front of the device. Each mirror is

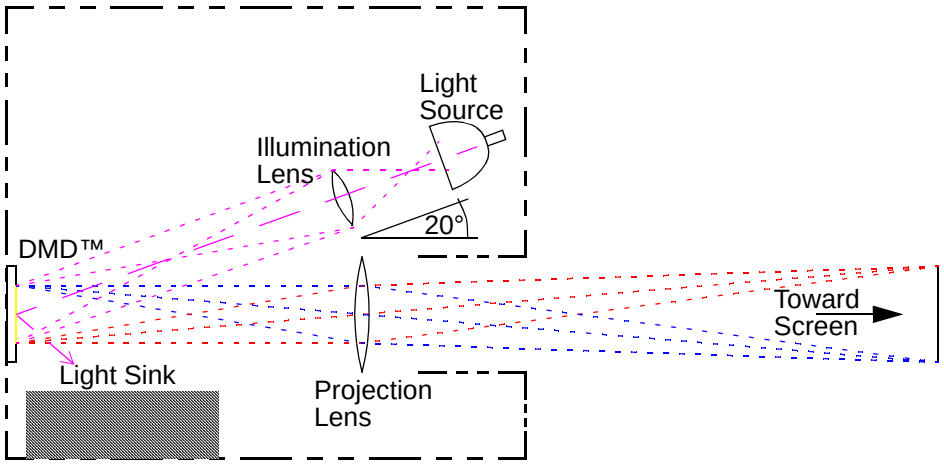


Figure 1.3 DMD™ projector optics

a pixel, and has two active positions, “on” and “off.” In the “on” position, a mirror tilts 10° toward the light source, and the incident light from the source is reflected into the projection lens. In the “off” position, the mirror tilts 10° away from the light source, reflecting the incident light away from the projection lens and into a light sink as shown in Figure 1.4. The projection lens still images the array onto the screen, but the “on” pixels are bright and the “off” pixels are dark.

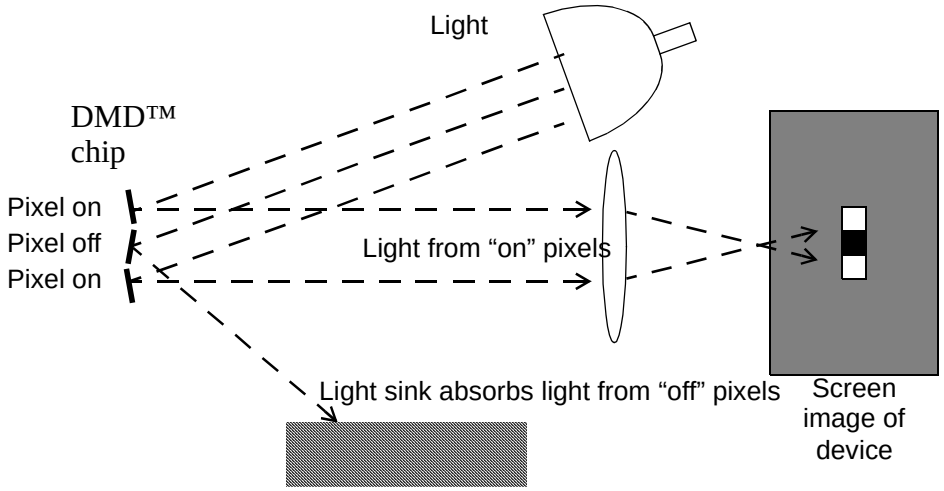


Figure 1.4 Individual pixel mirrors tilted in on and off positions

So far, we have a black-and-white image on the screen. Each pixel is either “on,” reflecting the white light from the source into the lens and is imaged as a white square, or the pixel is “off” and the corresponding square on the screen is dark. In order to form grey-scale images, we need to pulse-width modulate the light by rapidly moving the individual mirrors. To do this efficiently in a digital system, the brightness of each pixel is coded into a binary value that is typically eight bits long, representing the decimal values 0 to 255 as shown in Figure 1.5. If we think about this in terms of video, or an image that changes

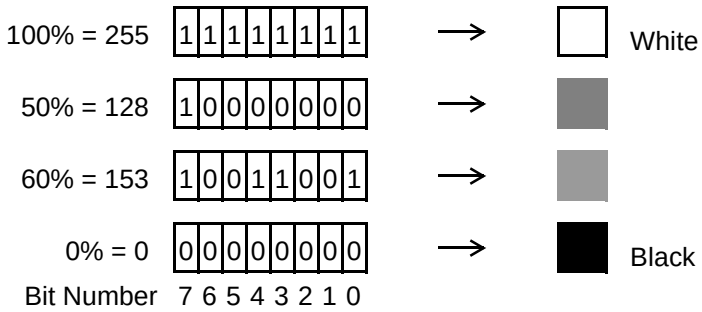


Figure 1.5 Grey-scale coding in binary numbers

many times per second, each image is displayed on the screen for one frame time. If we divide the frame time into 255 equal time slices, then we can associate a contiguous group of slices with each bit in the binary value. The least significant bit (bit 0) will be associated with the first time slice, the next bit (bit 1) will be associated with two slices, slice 2 and 3, and so on, with bit *n* associated with 2^n slices beginning with slice number 2^n. These eight groups will be turned on or off as a group, corresponding to the value in the associated bit

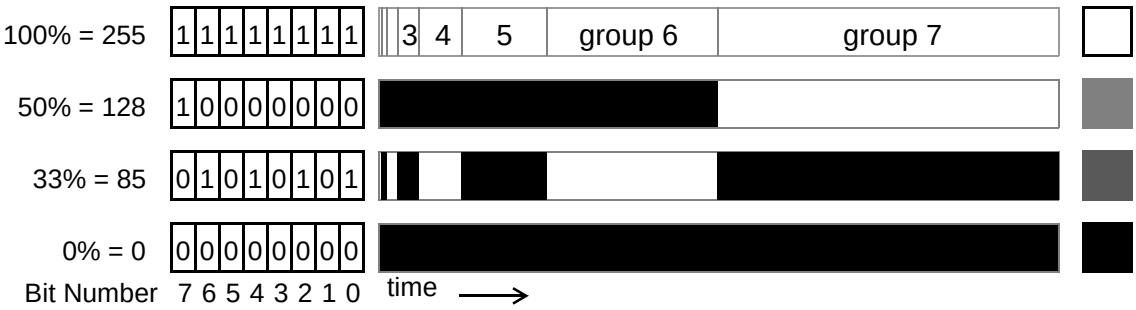


Figure 1.6 Translating grey-scale coding from binary numbers into pulse-width-modulated light streams

as is shown in Figure 1.6. A similar technique is described in a Sony patent[38]. Note that the image stays digital all the way to your eye, where the light from each pixel on the screen is focused on your retina and integrated to the desired grey-scale value. This method is inherently more accurate at delivering a grey value than any phosphor or liquid-crystal method, so long as the frame time does not exceed the flicker threshold of the eye. This threshold is approximately 20 ms.

How do we obtain color images? Texas Instruments' researchers have presented three methods to achieve color. The first and least expensive of these is to further subdivide the frame time and to sequentially present the primary colors using a white light source and a rotating color-filter-wheel, as seen in Figure 1.7. The second method is the most expensive, but it has the highest light efficiency. Three DMD™ chips are used, and a complicated glass prism system separates white light into red, green and blue components.

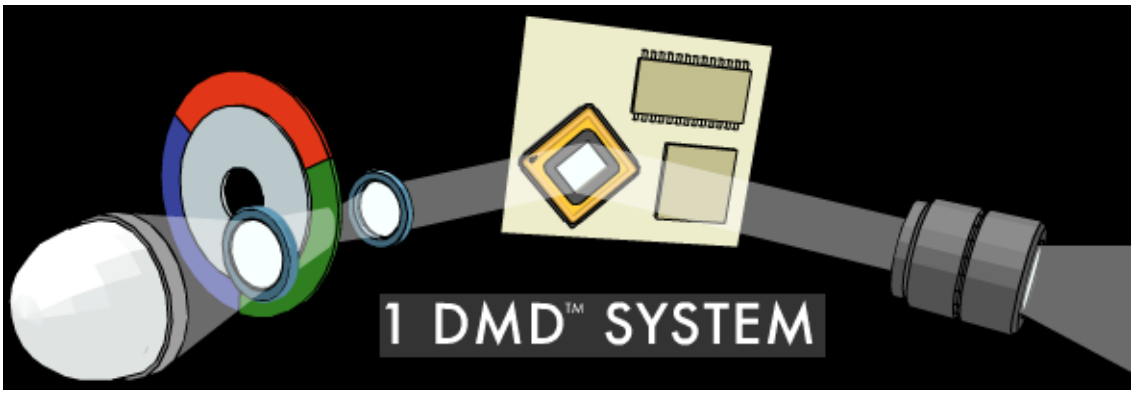


Figure 1.7 Color-filter-wheel concept to achieve full-color images
Graphic courtesy of Texas Instruments, Inc.

These components are each directed into a DMD™ chip at the required 20° angle, and the normal reflections from the three chips are combined into a full-color image. This prism system is illustrated in Figure 1.8. The third method is a compromise between the first

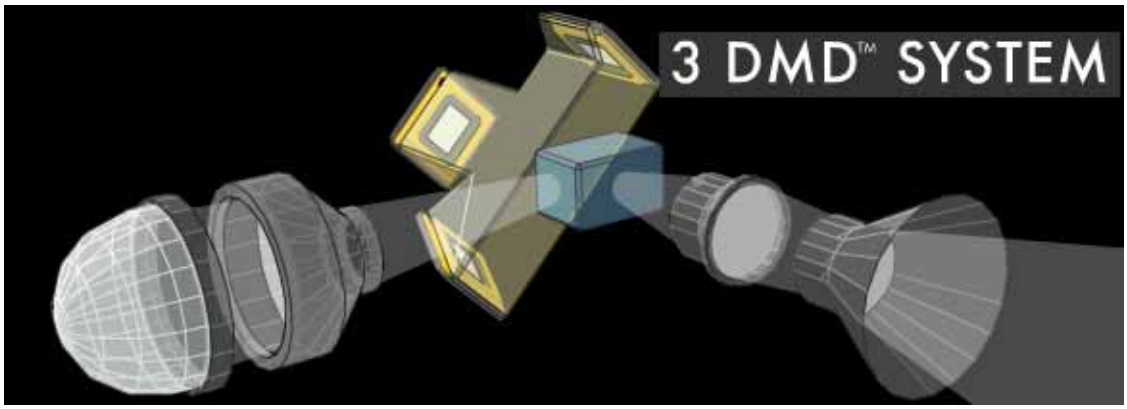


Figure 1.8 Full-color system concept with three micromirror chips
Graphic courtesy of Texas Instruments, Inc.

two: it uses both a prism system and a color-wheel, but only two DMD™ devices. The color-wheel is divided into yellow and magenta halves. The filtered yellow light is the combination of red and green light, and magenta is the combination of blue and red light. The prism separates the red component out of each of these and sends it to one chip; the remaining green or blue light is sent to the other chip. This yields increased optical efficiency, since each of the blue and green colors is available 50% of the time, instead of

33% of the time, as in the first method. This method also allows the use of a very long-life, inexpensive light source that is deficient in red light. Figure 1.9 shows the light paths used in each of the three methods.

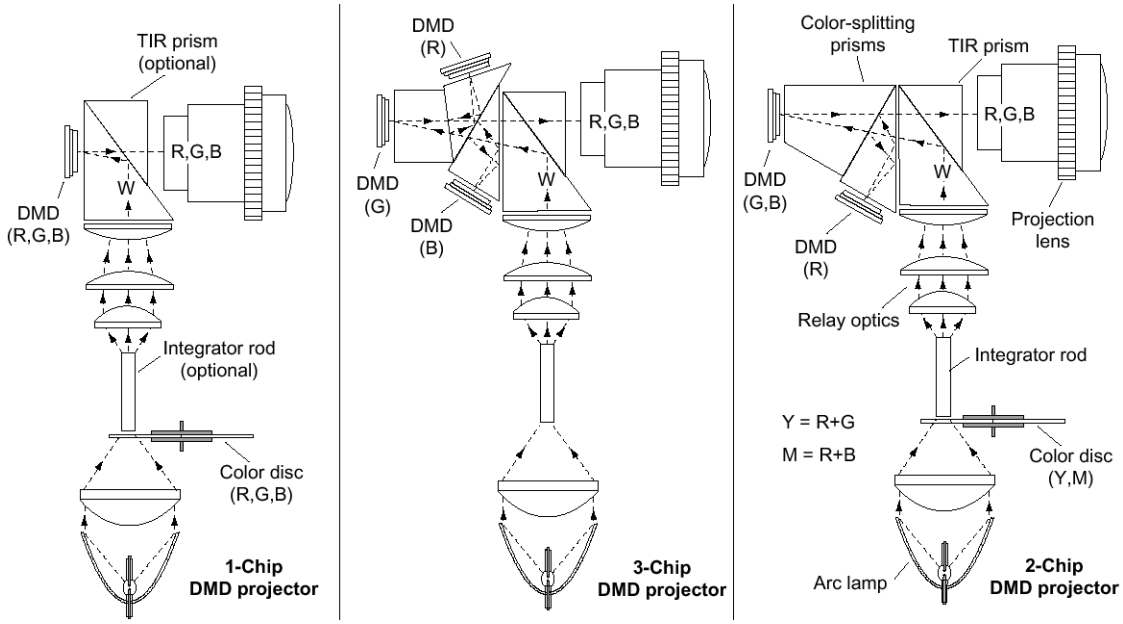


Figure 1.9 Optical paths for each of TI's methods for implementing color projection

Graphic courtesy of Texas Instruments, Inc.

1.3 Texas Instruments' Devices

Figure 1.10 shows an array of mirrors from the first working full-color device, operational in May of 1992. A single pixel is shown in Figure 1.11. A side view looking

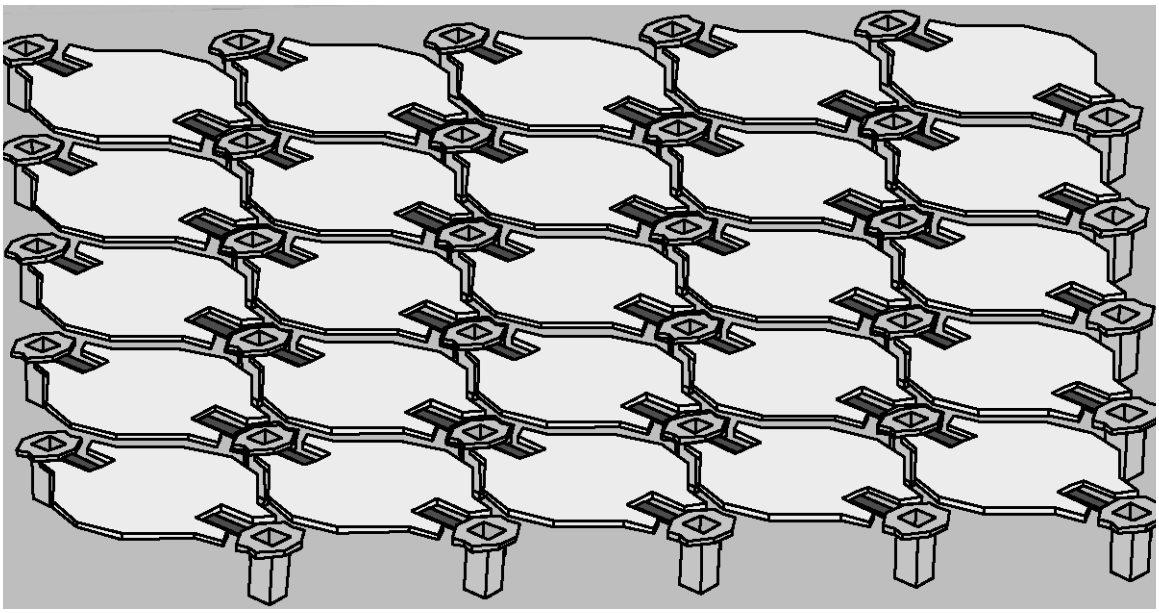


Figure 1.10 A portion of the first full-color DMD™ device
Graphic courtesy of Texas Instruments, Inc.[16]

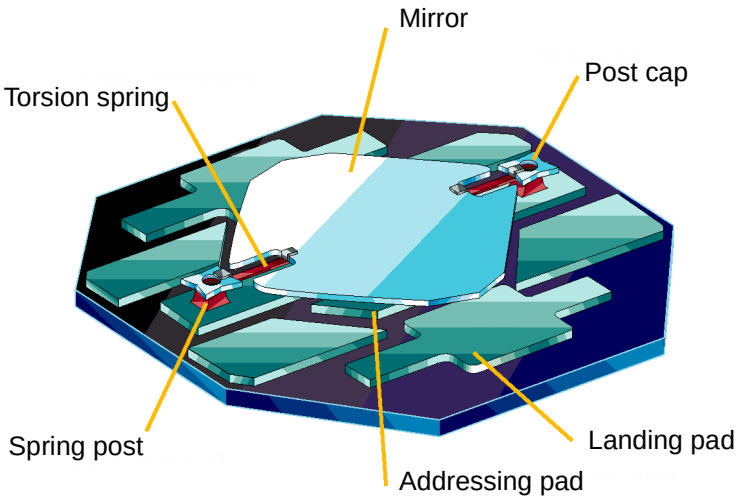


Figure 1.11 Components of a single pixel
Graphic courtesy of Texas Instruments, Inc.

along the torsion spring in Figure 1.12 shows the addressing pads and the landing pads. Addressing voltages are applied to the address pads from the underlying 5-volt CMOS memory cell. These voltages are complementary logic levels — that is, one is +5V and the other 0V with respect to the substrate. The mirrors and the landing pads are supplied with a (usually negative) bias voltage that changes during the addressing cycle.

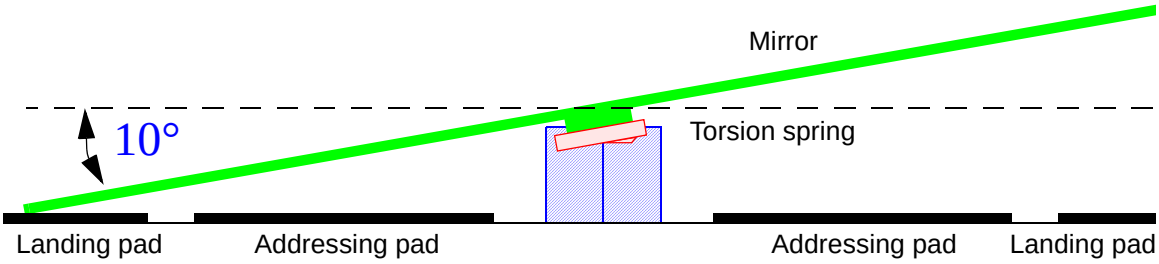


Figure 1.12 Side view of pixel

To pull the mirror down to the left-hand landing pad as shown, the addressing pad on the left side is driven to +5V and the one on the right to 0V. The bias voltage on the mirror is initially zero. The mirror starts to tilt toward the +5V side due to the electrostatic attraction. However, the spring force is too high to allow the mirror to move very far, and so a negative bias voltage in the range of -20V is applied to the mirror. This increases the attractive forces on both sides of the mirror, but more so on the left side that is already closer to its addressing pad, causing the mirror to snap down to the landing pad. The landing pad must be at the same potential as the mirror in order to prevent current from flowing through the contact point and welding the mirror to the landing pad.

These devices were described in an article that appeared in the IEEE *Spectrum* in November, 1993[39]. It was from that article that I first learned of this technology, and started thinking about ways to improve it.

There were four immediate problems that I wanted to address:

1. The springs were visible from the top of the array. I wanted to hide them underneath the mirror to increase the optical contrast ratio.

2. It looked like there would be a problem of metal fatigue in the springs. They were being made of aluminum, and I felt sure, at the time, that there would be a longevity problem with them.
3. I felt that the sticking mirror problem was caused by contacting aluminum mirrors onto aluminum landing pads. This process is a form of "stiction."
4. I disliked the color-wheel method. I knew from my previous industrial experience that there would be visible artifacts under specific viewing conditions due to the field-sequential color.

Of course, while I was off at Berkeley working on these problems, TI was not resting. They came out with a series of improved devices in the intervening years, as presented in Figure 1.13. They have published and presented frequently[40]-[46], and their

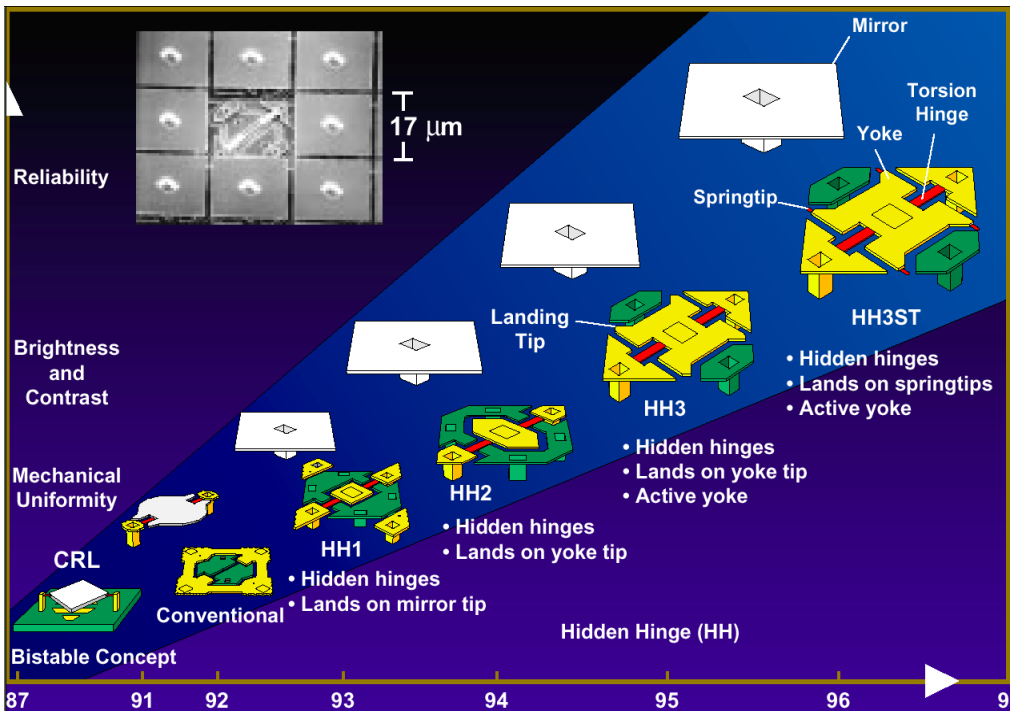


Figure 1.13 Evolution of the DMD™ pixel architecture
Image courtesy of Texas Instruments, Inc.

patent activity has been extensive[47]-[71].

TI attacked the contrast problem by hiding the “hinges” (that I call “torsion springs”). Their approach was quite similar to what I proposed to my qualifying exam committee in 1995. The result can be seen in their so-called HH1 device in Figure 1.13. They went after the fatigue problem with a metal alloy that still seems to be a trade secret. They appear to have solved the stiction problem with a series of devices and drive signal tricks. The improved devices, HH2, HH3, and HH3ST, as shown in Figures 1.13-1.17, are all improvements that reduced the stiction problem. In addition to the visible changes, they have used a surface monolayer applied in vapor form to further reduce the stiction.

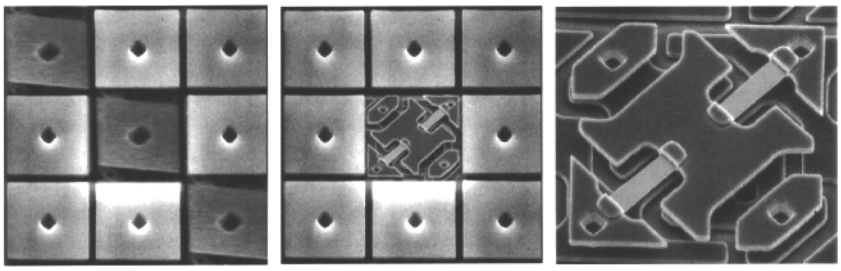


Figure 1.14 Micrographs of HH3 pixels
Image courtesy of Texas Instruments, Inc.

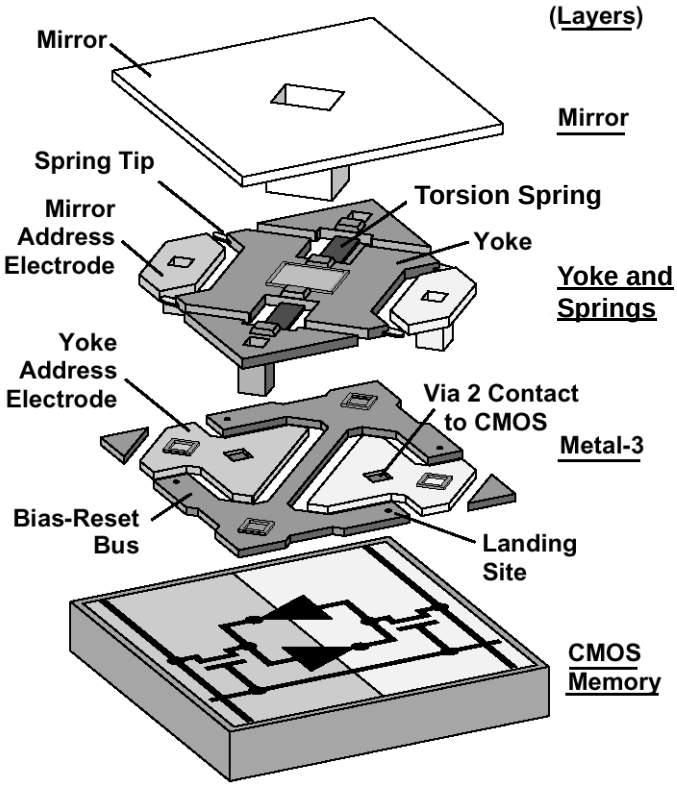


Figure 1.15 Exploded view of the layers of TI's pixel
Graphic courtesy of Texas Instruments, Inc.

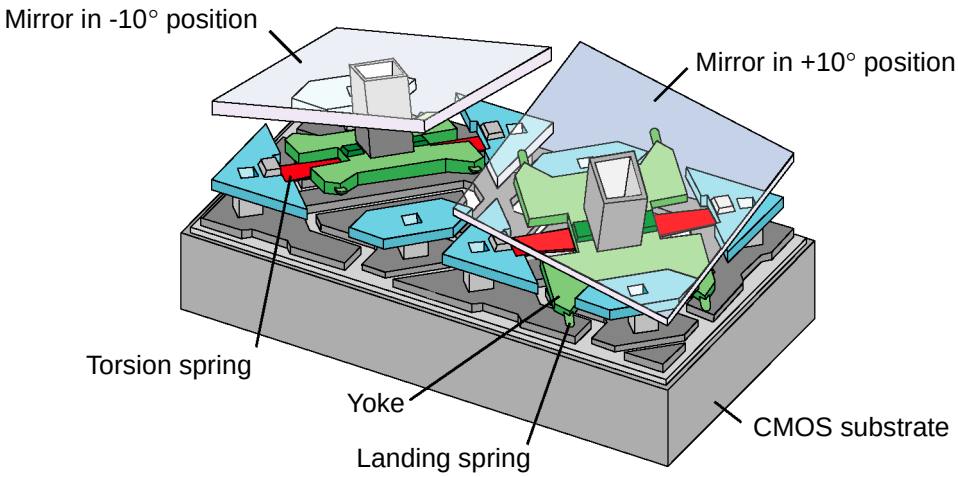


Figure 1.16 Two pixels shown in operating positions
Graphic courtesy of Texas Instruments, Inc.

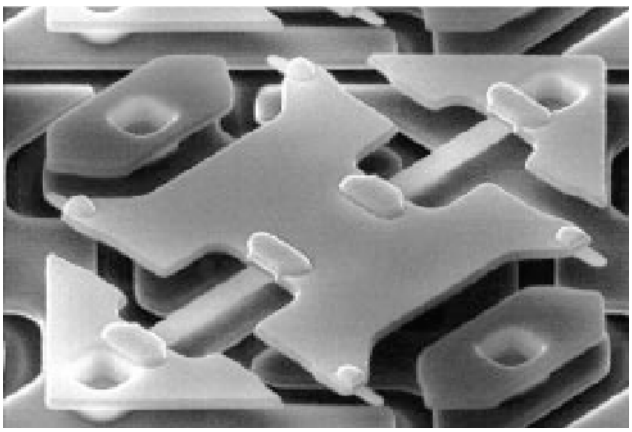


Figure 1.17 Micrograph of HH3ST pixel without the mirror
Note the spring tips on the ends of the yoke.
Image courtesy of Texas Instruments, Inc.

Since 1997, TI has further increased the contrast by decreasing the spacing between pixels, making the post in the center of the mirror smaller, and rotating the post 45° to reduce stray reflections into the lens.

The one remaining device problem is that the springs can take on a “set” if they are operated to one side for more than 95% of the time. This problem has been addressed by TI by enforcing a drive algorithm that guarantees that no spring will be driven in one direction with more than 95% duty cycle. The MTBF of the TI devices is now reportedly more than 100,000 hours if they are kept below 43°C while operating (see Figure 1.18). Finally, TI has addressed the sequential color problem with a three-chip projector system that they are marketing to the movie industry as the next generation of entertainment projectors (see Figure 1.19).

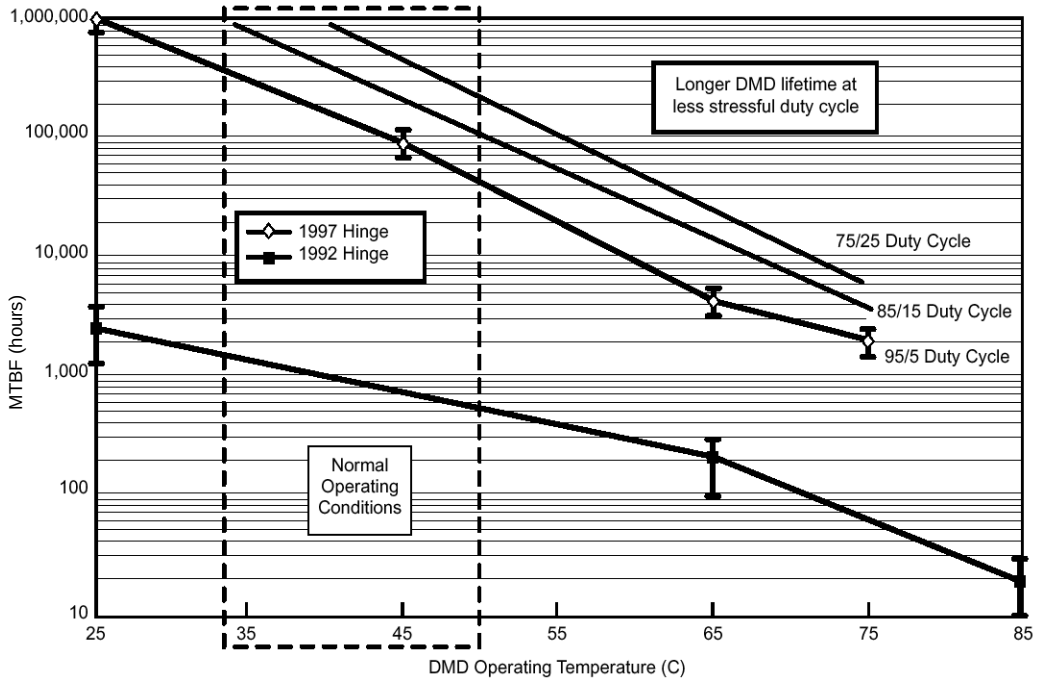


Figure 1.18 DMD™ chip estimated lifetimes vs. temperature for old and new spring materials operating at high duty cycles
Graphic courtesy of Texas Instruments Inc.[72].

Figure 1.19 Digital Light Processing™ cinema projector attached to a standard lamp housing
Image courtesy Texas Instruments, Inc.

TI has successfully transferred the manufacturing of these devices to one of their standard CMOS plants. They have three resolutions of chips available for OEM manufac-

turers (see Figure 1.20). With dozens of projector and television makers with products either available now or in the works, this technology appears to be headed for long-term success.

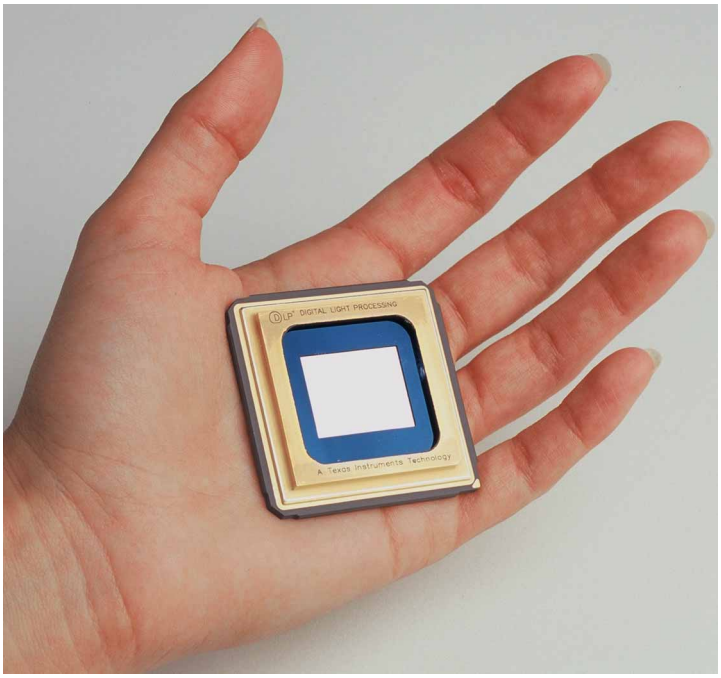


Figure 1.20 1280×1024 resolution DMD™ chip
Active area is 2.18cm × 1.74cm.
Image courtesy Texas Instruments, Inc.

2. Concept

2.1 Perceived Problems

On first seeing the *Spectrum* article[39] about the digital micromirror device (DMD), I was intrigued and delighted with the technology; however, several problems became immediately apparent to me.

First was the lifetime of the torsion springs in the device. These were being fabricated out of aluminum, and were naturally going to wear out through fatigue. Even today's devices still exhibit the problem of "taking a set." If the device is operated with greater than 95% duty cycle (favoring one side over the other) over a long period of time, then the spring will not return the mirror to a level position. This renders the mirror unusable, effectively shortening the life of the display. I believed that if these springs could be fabricated out of polysilicon, the life could be essentially unlimited since polysilicon has not exhibited fatigue when its strain is limited.

Second, the springs in TI's devices were being fabricated in the plane of the mirrors, which necessitated making notches in the mirrors and thereby reducing the effective efficiency and contrast. It was apparent to me that the springs should be hidden in a layer underneath the mirrors to allow the mirrors to be of maximum size and the springs to be slightly longer and therefore subject to less strain.

Third, there was a problem with mirrors sticking, which I attributed to their being made of aluminum. I thought that using polysilicon would help with this problem, or that perhaps the self-assembled monolayers that Michael Houston[73] had developed could prevent stiction.

Fourth and most intriguing were the methods used to turn what is inherently a monochrome device into a full-color display. The TI authors presented two alternatives, both of which looked problematic to me. The better of the methods, for both efficiency

and image quality, is the triple-chip method, which requires a separate chip for each primary light color. Systems made using this method combine three overlaid images to form the full-color image. Such three-chip systems are currently being installed into a number of theaters to replace film projectors. The downside to this is the expense of three chips, a complex prism system for combining the images (or three projection lenses), and the need to converge the three images by aligning chips or optics. These units will not be cost-competitive in high-volume markets like home theater and computer displays.

The second method presented for realizing full-color projection is time-division multiplexing of a single device using a rotating color wheel to filter a broadband light source to sequentially supply the primary light colors. This has several disadvantages. Most obvious is the low light efficiency, since most of the light is being absorbed by the color filter wheel at any time. This method also necessitates turning all the mirrors to the "off" position during the transitions of the color wheel, which forces some rather unnatural interruptions into the display-refreshing algorithms. What this means is that the device requires that a memory cell be built beneath each mirror to allow rapid loading of a pattern.

Finally, this method can create a nasty visual side effect that I call "motion color separation." This effect will occur whenever the observer's eye is tracking a moving object across the display screen, and the moving object's color is composed of more than one primary color. The problem cannot be corrected by image processing unless you can predict the behavior of the observer, which seems unlikely. To understand the nature of this phenomenon, you need to think about the rotation of the eyes while the observer tracks the image of a moving object across the screen. The eyes will move at a remarkably constant angular velocity, tracking the object very precisely. It is this constant velocity that gives rise to the apparent separation of time-division multiplexed colors.

I first observed a related visual effect that has the same basic cause in a vacuum-fluorescent display system that I was designing. The individual phosphor dots of the unit were rather large and spaced relatively far apart as shown in Figure 2.1. The display

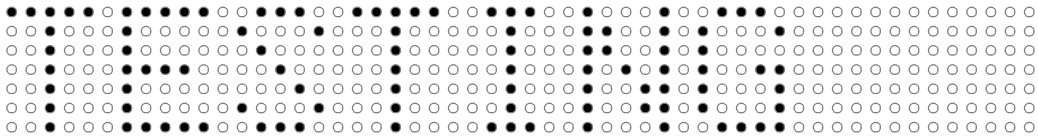


Figure 2.1 Display phosphor dot pattern

needed to be refreshed as the characters were time-division multiplexed. When text was scrolled rapidly across the screen, such that the motion was synchronized with the refresh frequency, the resultant motion appeared to be smooth. In other words, if the text was moved exactly an integral number of dots between successive refresh scans, the motion would appear to be smooth. Unfortunately, even when that number was one, the speed was too high for the average user to read comfortably, so I slowed the motion down by a factor of two by refreshing the image twice in each location before scrolling it to the next column. (I could not lower the refresh frequency because would have resulted in flicker.) When I did this, an amazing effect occurred — the apparent number of phosphor dots in the display doubled as shown in Figure 2.2. There appeared to be a new phosphor dot

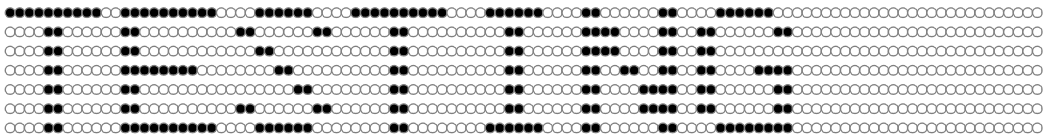


Figure 2.2 Apparent dot doubling while scrolling

between each horizontal pair of existing dots. This was at first quite troubling, but I soon discovered that if you didn't allow your eyes to track the moving message, the extra dots disappeared. I then realized that the observer's eyes were moving, and that when the dis-

play showed the same information on each pixel twice, the observer's eyes had moved on by a distance equal to exactly one-half of the pixel pitch. This meant that the second display of each dot would place the light at a different location on the observer's retina, a location separated by the one-half the pixel pitch as imaged on the retina.

This effect translates to a color-wheel-illuminated DMD in the following way. Suppose that we are viewing a tennis match in which a bright yellow ball is moving rapidly across a dark background. The yellow color is recreated using red and green light. If the image is presented first with a red image of the ball, followed by a green image of the ball, and the observer's eyes are not moving (because they are focused on a player or something stationary), the ball's image will be correctly reconstructed on the retina as yellow. If, however, the observer's eyes track the ball, then the two images (red and green) will be separated by some distance on the retina. If that distance is larger than the ball image, then the two colors will appear separately; otherwise, the image of the ball will have a red leading edge and a green trailing edge surrounding a yellow center, as shown in Figure 2.3.

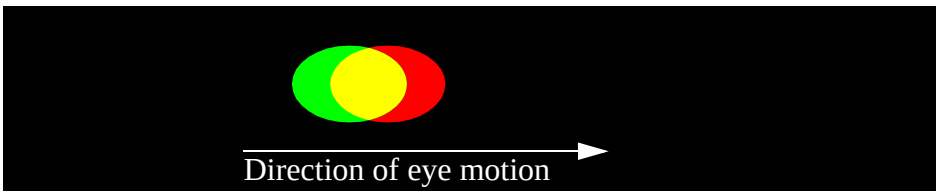


Figure 2.3 Motion color separation

It is possible to prevent this appearance in several ways, but in order to do so you must accurately predict the behavior of the observer's eyes. If you use a color frame-sequential camera, which scans out each color in the same order as the projection system is displaying it, then the image reconstruction should appear correct to the observer tracking the ball, but color-separated to the fixed-eye observer. Exotic image processing can be used to generate the same effect from a simultaneous-color camera, but again, without

prior knowledge of the observer's behavior, the image reconstruction cannot be correct for all observers.

I generated a small video of a bouncing white ball to demonstrate this phenomenon on a color-wheel DMD projector. (The effect cannot be observed on an ordinary color cathode-ray tube or liquid-crystal display.) If you have access to a color-wheel DMD display, and wish to see this effect, you can recreate this video by making sequential frames of a very small (five pixel diameter) white ball on a black background, and have the ball move four ball diameters between frames.

2.2 New Method for Generating Color Images

I was immediately intrigued with the idea of making a new type of DMD that would not require three separate chips, and that would operate without a color wheel. I began playing with equilateral triangle mirror shapes and soon found the following way to tile a plane with tilting mirrors. Each pixel would be made with three mirrors (instead of one), one for each primary light color — red, green and blue. Each of these mirrors would have its suspension oriented so that when the mirror is tilted into its active position, it would reflect into the projection or viewing lens only the light from the corresponding light source. To allow for maximum reflective surface area, each pixel would be fabricated in a hexagonal shape as shown in Figure 2.4. This would allow the image field to be tiled with a minimal separation between mirrors. The interior of a hexagon can be easily divided into six equilateral triangles, and so each diamond-shaped micromirror would consist of two adjacent triangles. The torsion spring that supports the mirror would lie under the line joining the center of the hexagon and the vertex of the hexagon located between the two triangles that form each mirror. The torsion spring would be placed below the mirror to allow the mirror to pivot without touching the spring or its supports.

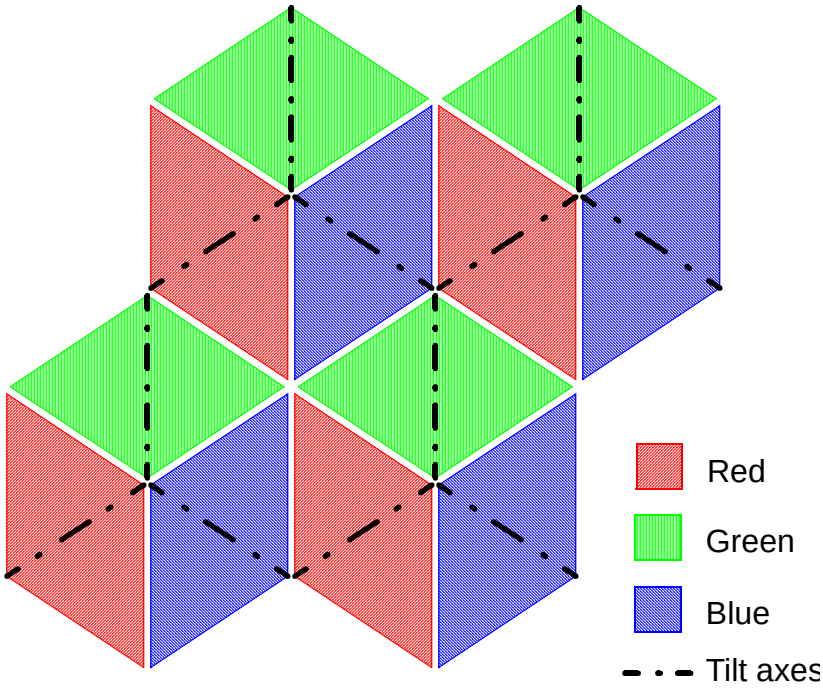


Figure 2.4 Hexagonal tiling of red, green and blue mirrors.

At this stage of the concept, I was still thinking about the array sitting on top of a static RAM array with one bit for each mirror. Much later came the realization that the memory cells were not required because of the electrostatic latch-up effect that allows a bias voltage to maintain the mirrors' position locked in either extreme. This memory effect allows one to use a refresh-by-row addressing scheme. Each row of hexagonal pixels needs a row conductor to bring all the mirrors and landing pads in the row to the same drive voltage. This voltage can be used to hold the positions of the mirrors while column electrodes associated with the pairs of electrodes under each mirror are changing in order to position mirrors in other rows.

During the initial design layout of the hexagonal device, I realized that the pixels could be square and that each mirror could be rectangular. The resulting pixels bear a very strong resemblance to the pixels of a liquid-crystal display. The individual mirrors for

each primary color still need to tilt on different axes. Figure 2.5 shows the individual mirrors and the lines of the underlying tilt axes.

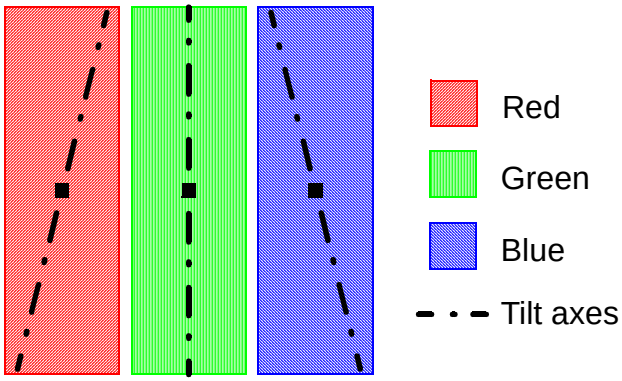


Figure 2.5 Square pixel tiling showing tilt axes.

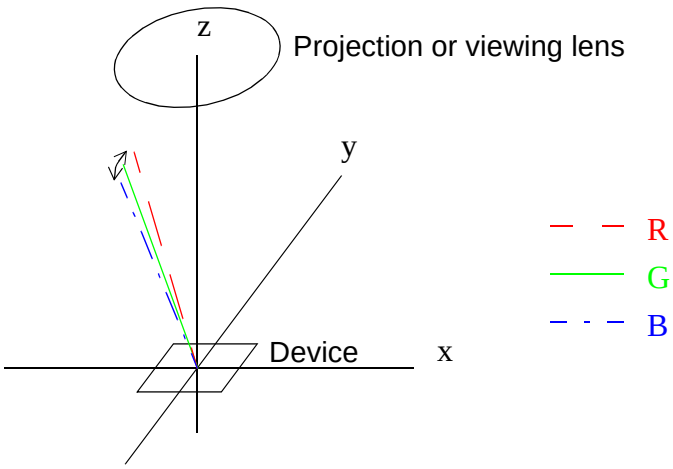


Figure 2.6 Direction of illumination sources

For viewing or projecting from a position directly in front of the chip, both of these possible tiling patterns require that the sources of the three primary colors of light be placed at angles that are twice the mirror deflection angle away from the normal to the surface. In addition, each source must be must be rotated about the normal from a position above the x-axis by the angle that the torsion spring makes with the y-axis, as shown in Figure 2.6. These source positions cause the reflections from “on” mirrors to be normal to the device and the reflections from “off” devices to be four times the mirror tilt angle away from the normal. The light sources used to illuminate one of these devices need not be three separate devices, but might be three dichroic mirrors that extract primary colors from a single white light source.

Reflections from mirrors that are “off” need to be absorbed by a light sink. While the design of such a sink is slightly outside the scope of this dissertation, a nice absorber might be found in the “black silicon” produced by over-etching a silicon wafer in a plasma etcher. The surface of black silicon consists of a forest of needle-like spikes that bounce light repeatedly down into the wafer, absorbing almost all of it.

3. Designs

Many design ideas are presented in this chapter. There are evolutionary ideas brought about by learning experiences in the fabrication process, and major leaps such as the switch from hexagonal to square pixels, or the switch to using an outside fabrication service. This chapter deals with translating these ideas into dimensions and processes.

3.1 Preliminary Design

My original concept for the tricolor device was based on the use of hexagonal pixels. That pixel design presented a small problem that comes from the hexagon itself. Most digital images, and high-definition television images employ square pixels. These square pixels mean the horizontal and vertical pixel pitches need to be equal in order to display the image without stretching. This problem and its solution are shown in Figure 3.1. Tiled hexagons have a horizontal pitch that is approximately 1.15 times the vertical pitch. If the radius of a circle circumscribing the hexagon is *R*, then the vertical pitch is

$$R(3\sin 30^\circ) = \frac{3}{2}R \qquad 1$$

and the horizontal pitch is

$$R(2\cos 30^\circ) \approx 1.732R\,. \qquad 2$$

The pitch ratio thus becomes

$$\frac{R(2\cos 30^\circ)}{R(3\sin 30^\circ)} = \frac{2}{3}\frac{1}{\tan 30^\circ} \approx 1.15\,. \qquad 3$$

To squeeze the pattern horizontally until the ratio is one, we can let the vertical edges be *R* and assume the horizontal pitch (*hp*) to be equal to the vertical pitch and solve for the angles of the non-vertical edges:

$$\left(\tan(\Theta) = \frac{\frac{1}{2}R}{\frac{hp}{2}} = \frac{R}{\frac{3}{2}R} = \frac{2}{3} \right) \rightarrow \Theta \approx 33.69° \qquad 4$$

This looks like a difficult layout problem until you realize that the endpoints of all the lines can all be placed on a regular grid, as shown in Figure 3.1. The slopes of the lines are ± 2/3.

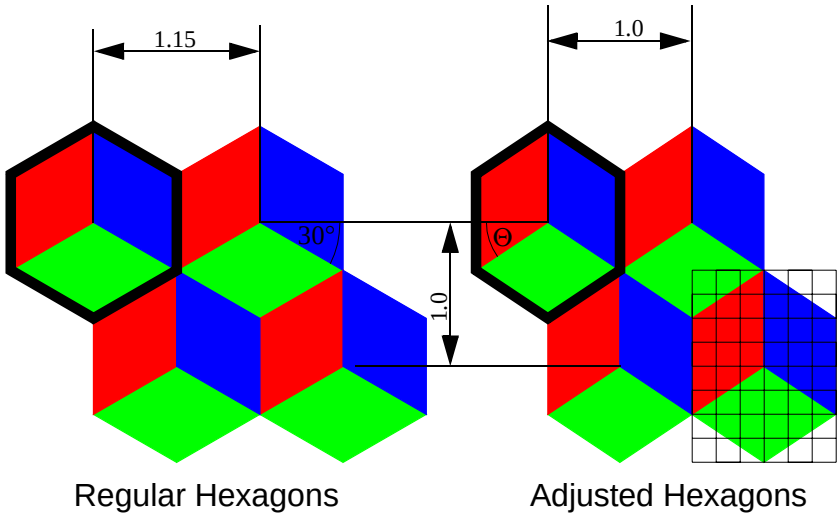


Figure 3.1 Aspect ratio adjustment
The small grid shows how the pattern fits well on a square grid.

Because the tips of the mirrors make contact with a landing pad to stop their motion (in this design), the pads need to be at the same electrical potential as the mirror is to prevent any current flow that might weld the tip down. In my designs, these landing pads are formed from the same film as the addressing pads. The mask layout for the hexagonal pixel is shown in Figure 3.2. The layout has 2.0-micron design rules and a pixel pitch of 48 microns and results in torsion springs on the red and blue mirrors that are almost exactly 7 microns long, while the springs on the green mirrors are 9 microns long.

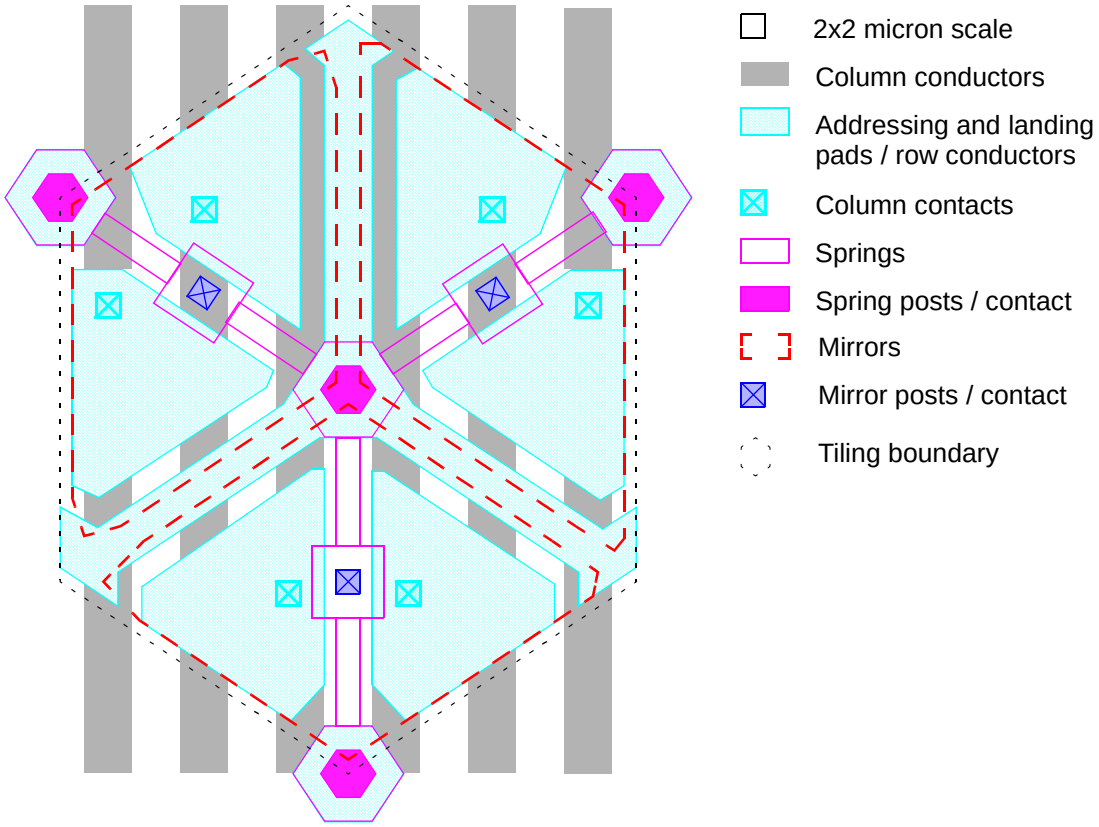


Figure 3.2 Layout of the pitch-corrected hexagonal pixel.
Note the absence of landing yokes and springs.

The row conductors also serve as the landing pads for the mirrors in this design. The post in the center of the pixel provides electrical contact to the springs (which must be conductive), and thus to the mirrors. All three posts at the edge of the pixel are shared with other rows, and thus the springs that contact those posts must not connect to each other to allow the row conductors to operate at different voltages. To achieve this, one may selectively dope the polysilicon used for the torsion springs to make only the central spring conductive. Another way to achieve the row isolation would be to insulate the tops of the outer posts with a nitride film before depositing the spring film. Yet another way would be to avoid sharing posts between rows by changing the layout and shortening the springs of

the “green” mirrors. Ideally, the resonant frequencies of the all the mirrors should match, and adjusting the lengths of the green mirror springs could accomplish this.

One of the interesting problems that arises in the hexagonal pixel design comes from tiling. When you tile the hexagons, the column conductors connect to one set of addressing pads in the odd rows and a different set in the even rows. We label the column conductors in Figure 3.2 from left to right, Red Left, Red Right, Green Left, Green Right, Blue Left and Blue Right. When these connect to the next row up or down, the Red Left conductors connect to the Green Right conductors. The Red Rights connect to Blue Lefts, and so forth. This is all due to the way the hexagons on the adjacent rows are offset by half the pixel width. All of the connections have shifted over three conductors, but since the signals will likely be driven by a shift register at the edge of the array, the difference is only three extra shifts, and this will allow the simple column conductor layout shown to work.

Another small problem with this design is that, because every other row of pixels is offset by one-half a pixel pitch, some signal processing will be required to shift the image on those lines by one-half a pixel. With analog source material, like NTSC, this is accomplished be shifting the sampling window by one-half pixel in time. With digital source material, this can be easily accomplished by averaging the individual RGB values of neighboring pixels, as shown in Figure 3.3. This requires an extra pixel in alternate rows as illustrated in Figure 3.3.

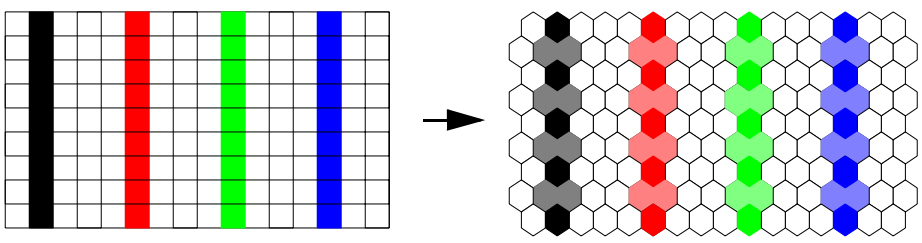


Figure 3.3 Pixel averaging for hexagonal array.

This hexagonal design hasn't been fabricated, though its layout is complete, in the xKIC format, which directly translates into Figure 3.2. The square pixel design is superior to the hexagonal pixel design in many ways. The primary advantages are: the longer springs and thus lower actuation voltages for a given spring film thickness; and the better matching of the square pixel pattern with digital source materials.

3.2 Berkeley Microlab Designs

The designs for fabrication in the Berkeley Microlab are based on two-micron design rules that were developed for use on the lab's GCA wafer stepper. The overall dimensions for the pixels are chosen to allow all of the necessary features to be incorporated without violating the design rules. Two small limitations of the mask generator affect the design process. First, the rectangular flash-mask prevents truly acute angles from being formed. Features that require acute angles must be approximated with a series of rectangles, as illustrated in Figure 3.4. The second is the allowable rotation angles for the

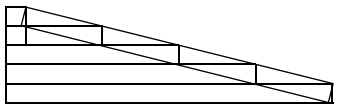


Figure 3.4 Approximating acute angles

rectangles, which are limited to increments of exactly 0.1°.

The xKIC layout editor imposes a number of constraints on the layout process. While the editor supports circles, arcs, boxes ("Manhattan" rectangles with sides parallel to the co-ordinate axes) and arbitrary polygons, the translator, which prepares the input for the pattern generator, ignores circles, and will only translate polygons with exactly four points that lie on the corners of a rotated rectangle. Since xKIC uses five points in the polygonal rectangles it generates for arcs, with the last point exactly matching the first, arcs require manual editing to remove their fifth point. Since xKIC doesn't directly support rotations of other than 90 degrees, I use a Mathcad function that I call "Rotbox," (see

"MathCad Sheets" on page 55) that generates the co-ordinates of the polygon structures supported by xKIC to represent a rotated rectangle. Structures in the design that appear to be polygons are actually manually overlaid boxes and rotated rectangles.

Figure 3.5 shows the layout of the first of the square pixel designs. The overall dimensions are 60 microns by 60 microns. Column conductors of doped polysilicon run underneath the pixel. The surface is planarized to the top of these conductors using deposited low-temperature silicon-dioxide (LTO) and chemical mechanical polishing (CMP). The LTO is protected with a thin layer of silicon nitride, so that it will not be removed in the final release etch. Contact holes for the address pads are etched through to the column conductors. The next layer of doped polysilicon forms the addressing pads (that will have charges placed on them to attract the mirrors), row conductors and landing pads. After again planarizing the surface, depositing a sacrificial LTO layer whose thickness is one-half of the vertical spacing between the mirrors and the addressing pads, and etching contact holes to the row conductors, the next polysilicon layer forms the yokes and spring anchors, which are stiff structures to which the thin springs attach. This is followed directly by the very thin layer of doped polysilicon that forms the torsion and touchdown springs. Notice that the 1.0μm springs deliberately break the 2.0-micron design rule in this layout — this is to make softer springs. Other designs are more conservative. Another layer of sacrificial LTO is deposited and planarized to be the second half of the mirror gap, contacts to the yokes are etched, and the final doped polysilicon layer forms the mechanical base for the mirrors. After a light CMP to remove the surface roughness of the polysilicon, a layer of aluminum or gold may be deposited to improve mirror reflectivity.

The angles selected for the red and blue torsion springs are ±14° from the vertical. These angles were chosen in part because they can be laid out on a grid with a slope of 4 (arctangent(1/4) ≈ 14.036 degrees). The yokes and the contact holes to the yokes are rotated by the same angle as the springs. The yokes are rotated so that the contact torque is

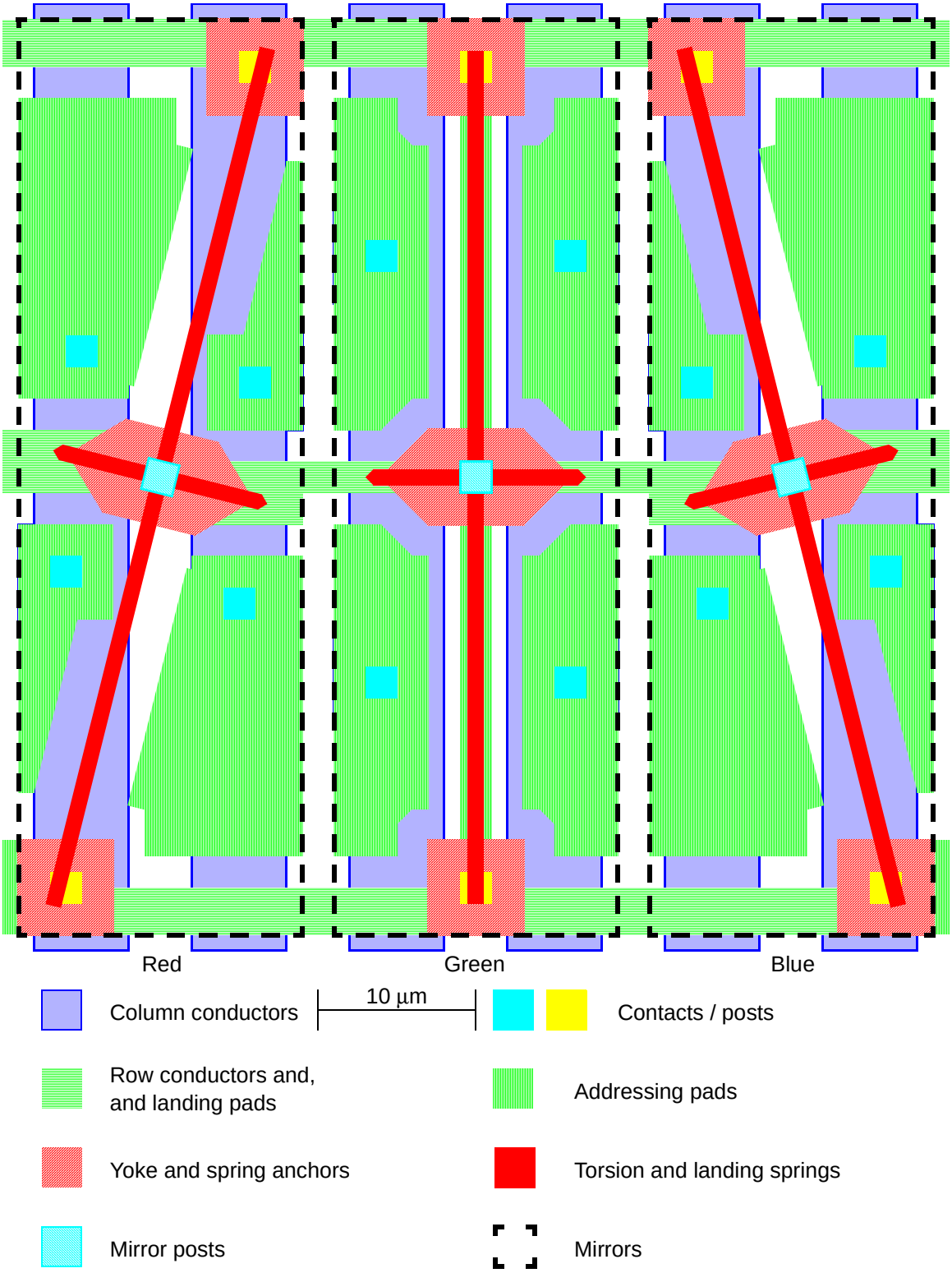


Figure 3.5 Pixel 1 layout — mirrors are shown in outline form to allow underlying layers to be seen.

balanced on the two halves of the torsion spring, and the contact holes are rotated so that the stray reflections from the edge of the hole in the center of the mirror will pick up the corresponding light source. In retrospect, these should be rotated another 45 degrees to avoid sending any reflections into the projection lens.

To determine the thickness of the torsion springs, we will go through a series of calculations:

1. We derive the required thicknesses for the sacrificial layers that separate the addressing electrodes (address pads) from the mirrors;
2. We calculate the capacitance between the address pads and the mirrors as a function of the mirror angle;
3. We determine the torque that results from an applied voltage as a function of the tilt angle; and finally
4. We find the torsional spring constant limit that will allow the calculation of the spring thickness.

We begin by selecting the maximum tilt angle of the mirrors. Since working devices had been made (at Texas Instruments, Inc.) using 10° mirror tilts, that number was selected as being large enough to keep the optical input and output components out of each other's way, while not being so large as to require a wastefully large spacing for tilting the mirrors. From the arrangement of the red and blue mirrors as shown in Figure 3.5, we see that the thickness, z_{mirror}, of the sacrificial layers that separate the bottom of a mirror from the landing/addressing layer is determined by the tilt angle and the largest perpendicular distance, R_{max}, of the mirror edge from the axis of rotation. Figure 3.6 shows the arrangement.

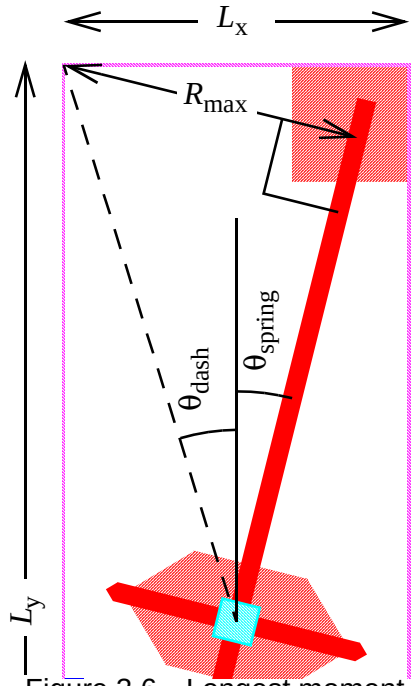


Figure 3.6 Longest moment arm, R_{max}

To determine R_{max}, first we find the length of the dashed line between the center and one corner of the mirror:

$$L_{dash} = \frac{1}{2}\sqrt{L_x^2 + L_y^2} = \frac{1}{2}\sqrt{18.0\mu m^2 + 58.0\mu m^2} \approx 30.4\mu m. \quad 5$$

Next, the angle between the dashed line and the y axis:

$$\theta_{dash} = \text{atan}\frac{L_x}{L_y} = \text{atan}\frac{18}{58} \approx 17.24°. \quad 6$$

To find the angle formed between the dashed line and the rotation axis (the center of the torsion spring), we add the 14° spring angle, θ_{spring}, to θ_{dash} and then we can find the length of the moment arm R_{max}:

$$R_{max} = L_{dash}\sin(\theta_{dash} + \theta_{spring}) \approx 15.75\mu m. \quad 7$$

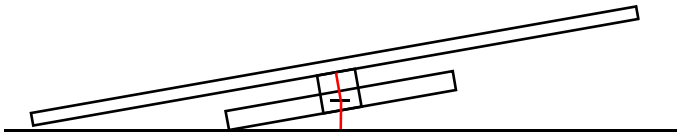


Figure 3.7 Tilted mirror showing post and landing yoke. The fabrication plane of the torsion spring is indicated by the dash

Figure 3.7 shows the mirror in its tilted position viewed along the rotational axis. Assuming that the corner of the mirror touches the landing pad, and that the torsion spring is located halfway between the mirror bottom and the landing surface, we use one-half of the maximum tilt angle, θ_{tilt}, and R_{max} to find z_{sp}, the height at which the spring should be fabricated:

$$z_{sp} = R_{max}\tan\left(\frac{\theta_{tilt}}{2}\right) \approx 1.38\mu m . \qquad 8$$

The minimum height for the bottom of the mirror is twice z_{sp}, but since the mirror isn't supposed to touch the landing pad, a small arbitrary separation distance (0.04μm) was added:

$$z_{mirror} = 2z_{sp} + 0.04\mu m \approx 2.8\mu m . \qquad 9$$

Calculating the correct dimensions for the cross-section of the torsion springs involves finding an approximation to the torque generated by electrostatic attraction as a function of the tilt angle and a reasonable actuation voltage, and then solving for a spring constant that will allow pull-in over most of the tilt range.

I made a conservative estimate of the attraction force between the mirror and one side of the addressing electrodes, by using only the area of the electrodes and assuming that the mirror has the same area. Attraction of the yoke to the address pads is ignored because the yoke is not above them. The actual addressing pads are in two pieces with the approximate shape of a triangle with a gap under the yoke. Thus, my estimate is based on integrating the areas of the triangle along the maximum perpendicular since both the capacitance and the torque will vary with distance from the axis of rotation. The effects of

the errors due to the pads not matching the triangle near the spring are minimized by the small radial distance, and hence small moment contribution there.

Figure 3.8 shows one triangle with its base parallel to the torsion spring, its height

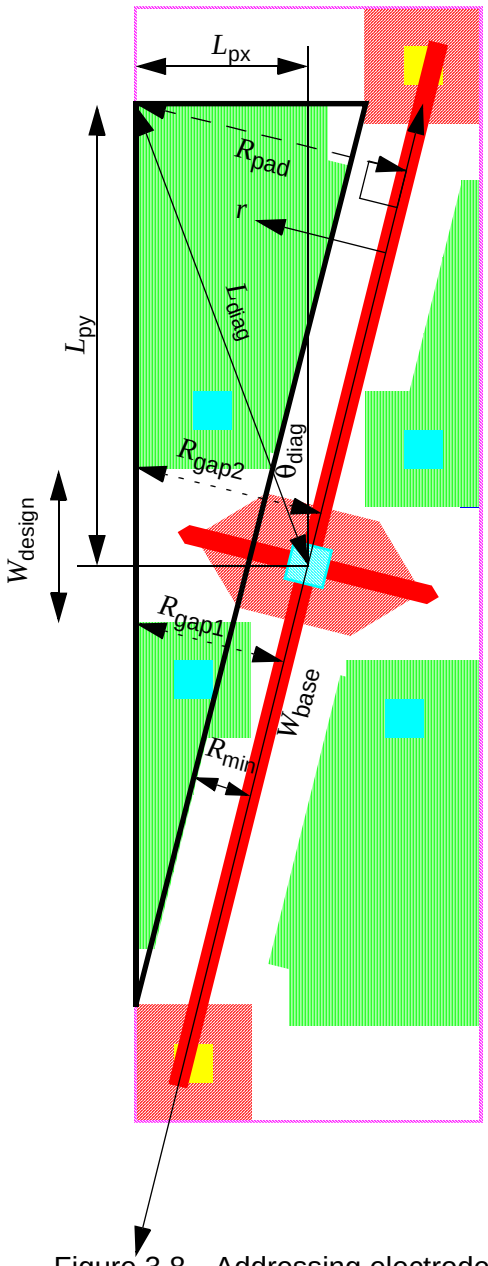


Figure 3.8 Addressing electrode geometry

indicated by a dashed line, and its gap radii indicated by dotted lines. Because the capacitance will depend on the distance between the plates, which is a function of the radius

from the axis of the torsion spring and the angle, we need a piecewise linear expression for the width of the triangle as a function of the radius from the torsion spring. The maximum radius from the spring axis to the corner of the addressing electrode, R_{pad}, is calculated just like R_{max} in equations 5 through 7:

$$L_{diag} = \sqrt{L_{px}^2 + L_{py}^2} = \sqrt{9.0\mu m^2 + 24.0\mu m^2}, \quad 10$$

$$\theta_{diag} = \operatorname{atan}\frac{L_{px}}{L_{py}} = \operatorname{atan}\frac{9}{24}, \quad 11$$

$$R_{pad} = L_{diag}\sin(\theta_{diag} + \theta_{spring}) \approx 14.5\mu m. \quad 12$$

The radii from the spring axis to the points where the gap in the electrode ends are calculated in the same manner. The results are $R_{gap2} \approx 10\mu m$ and $R_{gap1} \approx 8\mu m$. The minimum radius, R_{min} is just the distance from the spring axis to the baseline of the triangle that is set by the design at $3\mu m$. The base width of the triangle if it were extended all the way to the axis of the spring is given by:

$$W_{base} = \frac{L_{py}}{\cos\theta_{spring}} + \frac{L_{px}}{\sin\theta_{spring}} \approx 61.9\mu m, \quad 13$$

which will be useful in calculating the width of the triangle as a function of the radius. The gap width is $8.0\mu m$ along the y-axis, but since the triangle base is 14° off the y-axis, the effective width of the gap is given by:

$$W_{gap} = \frac{W_{design}}{\cos\theta_{spring}} = \frac{8.0\mu m}{\cos 14°} \approx 8.25\mu m. \quad 14$$

The resulting piecewise linear expression for the effective width of the triangle as a func-

tion of the radius is:

$$W_{\text{pad}}(r) = \begin{cases} \text{If } |r| < R_{\text{min}}, & 0 \\ \text{If } R_{\text{min}} < |r| < R_{\text{gap1}}, & \dfrac{R_{\text{pad}} - |r|}{R_{\text{pad}}} W_{\text{base}} - W_{\text{gap}} \\ \text{If } R_{\text{gap1}} < |r| < R_{\text{gap2}}, & \dfrac{R_{\text{pad}} - R_{\text{gap2}}}{R_{\text{pad}}} W_{\text{base}} \\ \text{If } R_{\text{gap2}} < |r| < R_{\text{pad}}, & \dfrac{R_{\text{pad}} - |r|}{R_{\text{pad}}} W_{\text{base}} \end{cases} . \quad 15$$

The absolute value of r is used so that torque can be calculated across the entire pixel if desired. It should be noted that for any shape of the addressing electrodes, there exists a similar piecewise expression for $W_{\text{pad}}(r)$ and a value for R_{pad} that could be carried forward through the rest of these calculations for any similar design.

The distance, d, which separates the plates of the capacitor formed by the mirror and the addressing electrodes, is a function of the radius, r, and the mirror angle, θ, is approximated by:

$$d(r, \theta) = z_{\text{mirror}} - 2r \tan\frac{\theta}{2}. \quad 16$$

The electric field strength at a given radius can be found by dividing the applied voltage by the distance:

$$E(r, \theta, v) = \frac{v}{d(r, \theta)} . \quad 17$$

The capacitance per delta of the radius is approximated by:

$$C(r, \theta) = \varepsilon_0 \frac{W_{\text{pad}}(r)}{d(r, \theta)} \Delta r . \quad 18$$

Integrating this over the radius gives us the capacitance as a function of the tilt angle:

$$C(\theta) = \varepsilon_0 \int_0^{R_{\text{pad}}} \frac{W_{\text{pad}}(r)}{d(r, \theta)} dr , \quad 19$$

giving a zero-tilt capacitance of:

$$C(0°) = 0.77\text{fF} \tag{20}$$

and a full-tilt capacitance of:

$$C(10°) \approx 1.6\text{fF}. \tag{21}$$

Thus, the capacitor charge per delta r is given by:

$$Q(r, \theta, v) = C(r, \theta)v. \tag{22}$$

This, combined with the field strength, gives us the force per delta r:

$$f(r, \theta, v) = E(r, \theta, v)Q(r, \theta, v) = \varepsilon_0 W_{\text{pad}}(r)\frac{v^2}{d(r, \theta)^2}\Delta r. \tag{23}$$

We can use this last expression to approximate the torque contributed for each delta r by multiplying the force by the radius:

$$T(r, \theta, v) = f(r, \theta, v)r = \varepsilon_0 W_{\text{pad}}(r)\frac{v^2}{d(r, \theta)^2} r\Delta r. \tag{24}$$

Finally, the net torque produced on the spring is approximated by integrating over the radius:

$$T(\theta, v) = \int_0^{R_{\text{pad}}} \frac{T}{\Delta r}(r, \theta, v)dr = \varepsilon_0 v^2 \int_0^{R_{\text{pad}}} W_{\text{pad}}(r)\frac{r}{d(r, \theta)^2}dr. \tag{25}$$

Figure 3.9.is a plot of Equation 25 for all allowed tilt angles with a five-volt potential between a mirror and one of its address electrodes.

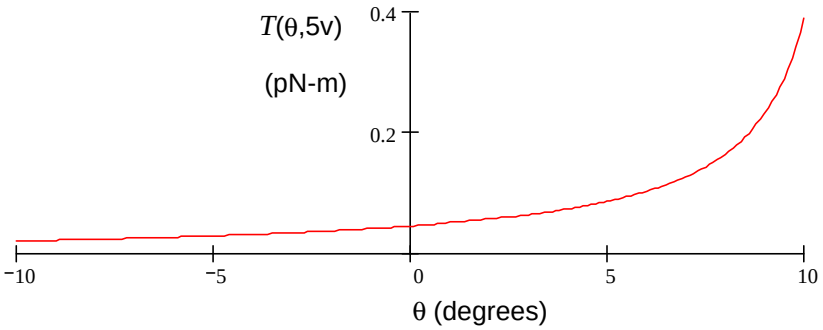


Figure 3.9 Electrostatic force versus mirror angle
assuming a +5V potential only on one address electrode with respect to the mirror

Next, we plot the torque from both address pads, assuming that one is at +5V, the other is at 0V and the mirror is at a bias potential of -15V (all with respect of the substrate). Under these conditions, there is a net attractive potential of 20V on one side versus 15V on the other. Figure 3.10 shows the net torque produced by both address pads when

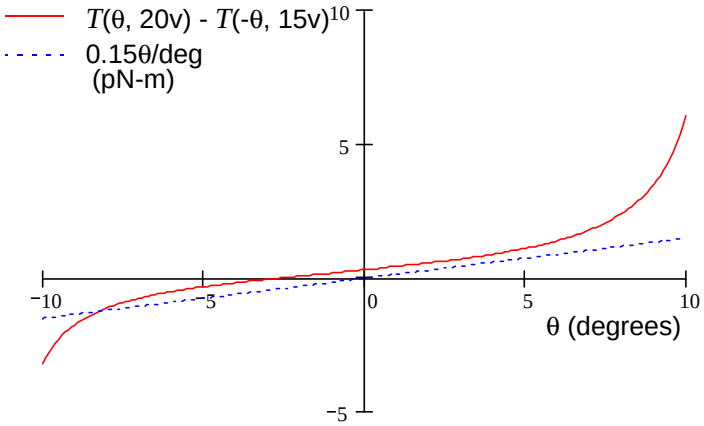


Figure 3.10 Torque vs. angle with +5V on one address electrode
and 0V on the other with -15V on the mirror (solid line).
A reasonable torque to balance with the torsion spring (dotted line).

the negative bias is applied to a mirror through its row conductor. In addition, a linear torque that could serve as an upper limit for selecting the spring constant is shown as a dotted line.

Assuming that the torsion spring has a linear spring constant K_Φ, we need to select K_Φ such that the restorative torque it produces will be less than the actuation torque at all positive and most of the negative angles.

The formula for the torque spring constant on a clamped-clamped rectangular beam from Roark[74] is:

$$K_\Phi = \frac{2}{l}(KG + \sigma J), \qquad 26$$

where l is the length of one-half of the spring, σ is Poisson's ratio for the material and J, G and K are given by:

$$J = \frac{1}{12}[ab^3 + a^3 b], \qquad 27$$

$$G = \frac{E}{2(1-v)}, \qquad 28$$

$$K = a^3 b\left[1 - \frac{192a}{\pi^5 b}\sum_n \frac{1}{n^5}\tanh\left(\frac{n\pi b}{2a}\right)\right], \qquad 29$$

where a is the smaller of the dimensions of the rectangular cross-section and b is the larger, E is Young's modulus for the material and v is a correction factor. Using 170GPa as E and 0.3GPa as σ for polysilicon, and setting b to 1.0μm, and l to 20μm (both from the pixel layout), we can solve for the spring thickness, a, given the spring constant. The required thickness is found to be 90nm. When we add the spring torque to the electrostatic torque curve we obtain Figure 3.11. Notice that the torque at -10° is sufficiently negative to hold a mirror in place even when the addressing voltages are set for the opposite position. In order to switch a mirror's position, the bias voltage must be removed long enough to accelerate the mirror past the zero crossing, which occurs at about -8°.

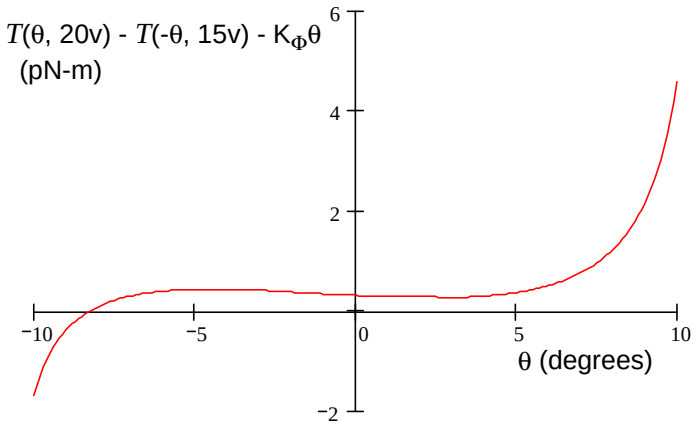


Figure 3.11 Net torque vs. angle with spring restoring torque included

3.3 Die layout

The pixels are tiled up in an array of 16 × 16 pixels (960 microns square) and connected to bonding pads for testing on two sides of the array. A minimum of six bonding pads are required to provide signals to the column conductors for one pixel, and the minimum practical size and spacing for bonding pads is 100 microns. Therefore, just one set of six pads (1100 microns wide) is shared by all the columns. Eight bonding pads (1500 microns tall) are connected to the rows so that each pad can activate two rows in the matrix for testing purposes. The resulting arrays are about 1.5 millimeters square, allowing twenty-four such arrays to be fabricated in a 9.1mm × 8.25mm die size as shown in Figure 3.12.

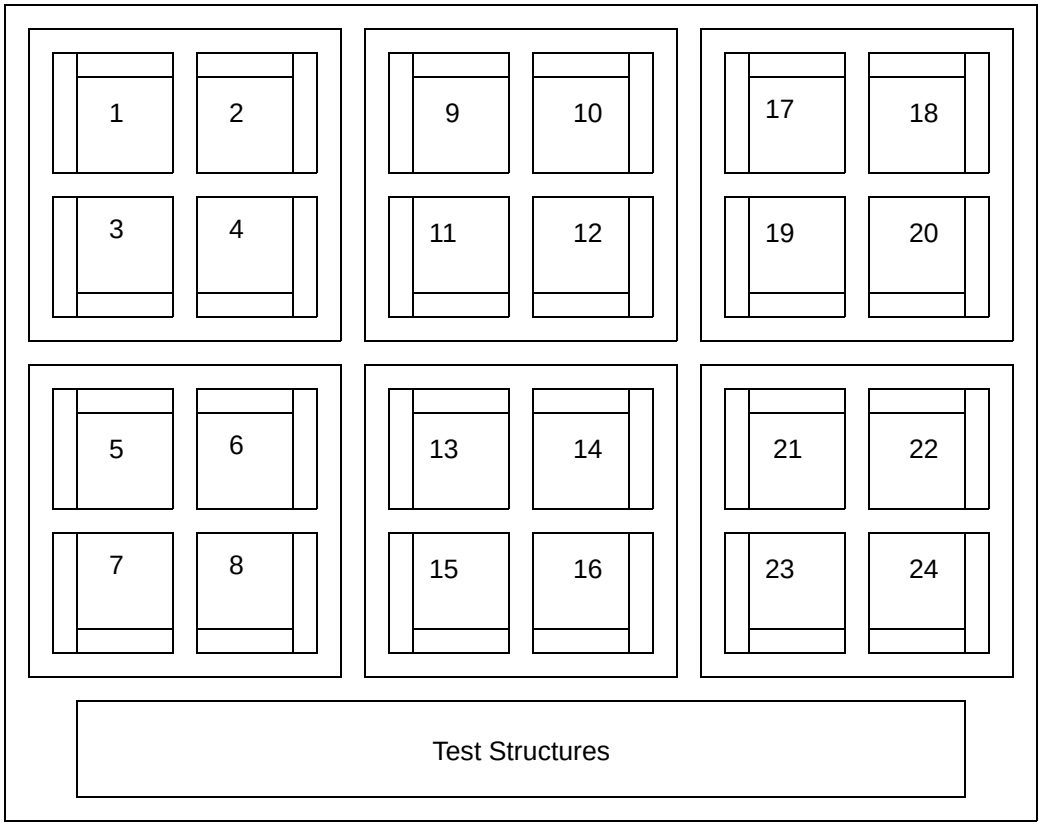


Figure 3.12 Overall die layout showing sub-die locations and their bond pad areas. The die measures 9.5mm by 8.1mm.

I refer to each matrix as a sub-die because it could be cut away from the rest of the structure for packaging and testing. Since bonding pads are placed on only two sides of each sub-die, four sub-die are grouped into a mini-chip that is surrounded by an etch-protection/sawing trench. Therefore, the group of four sub-die can be placed into a 56-lead package and completely wire bonded without having bond wires passing over any of the arrays.

Since so many mirror arrays fit on a die, I chose to explore the design space by varying each sub-die's mask. Table 3.1 summarizes the combinations of features that are designed into the masks. Stepped address pads are designed to decrease the voltages required to actuate and hold the mirrors. Areas on the addressing pads that are closer to the

torsion springs are made thicker than the rest of the pad (stepped) using an additional mask and an additional etching step. (After the first few runs, this layer was abandoned as it was unnecessarily increasing risk, and complicating the planarizing steps.) Another feature that is designed in but has not been tried is an insulating silicon nitride “bumper” added to the corners of the stepped addressing pads. Both of these features require an additional mask in the set, and were not included in the final process. Design variations included are: narrowing the torsion spring to one micron; eliminating the thick yoke layer (making the yoke using the spring film); adding Texas Instruments-style landing springs to the yokes; and using a pair of vertical stringers as the springs. The stringer springs use an additional mask and an etch step to form the trenches whose side walls are coated with the spring material. Stringers are formed when an anisotropic plasma etch removes the horizontal parts of the thin film and leaves the vertical parts.

Table 3.1 Design feature combinations.
An “x” indicates that the feature is designed into the sub-die.

Feature	Sub-Die Number																							
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Flat address pads	x	x	x	x	x	x	x	x																
Stepped pads									x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Insulated steps																	x	x	x	x	x	x	x	x
1µ spring	x				x				x				x				x				x			
2µ spring		x		x		x		x		x		x		x		x		x		x		x		x
Vertical spring			x				x				x				x				x				x	
Thick yoke	x			x	x			x	x			x	x			x	x			x	x			x
Landing springs	x	x	x	x					x	x	x	x					x	x	x	x				

Since the stepped pads and insulated steps aren’t incorporated into the chips that were fabricated, the net effect is that there are three copies of the first eight designs.

A pseudo-3D layout done in AutoCAD is presented for purposes of better visualization in Figures 3.13-3.15. Layers are positioned on the z-axis and extruded to give them thickness. The resulting 3-D models were given various degrees of transparency to allow the viewer to see through to underlying layers. Multiple light sources and shadows give the resulting renderings a realistic look.

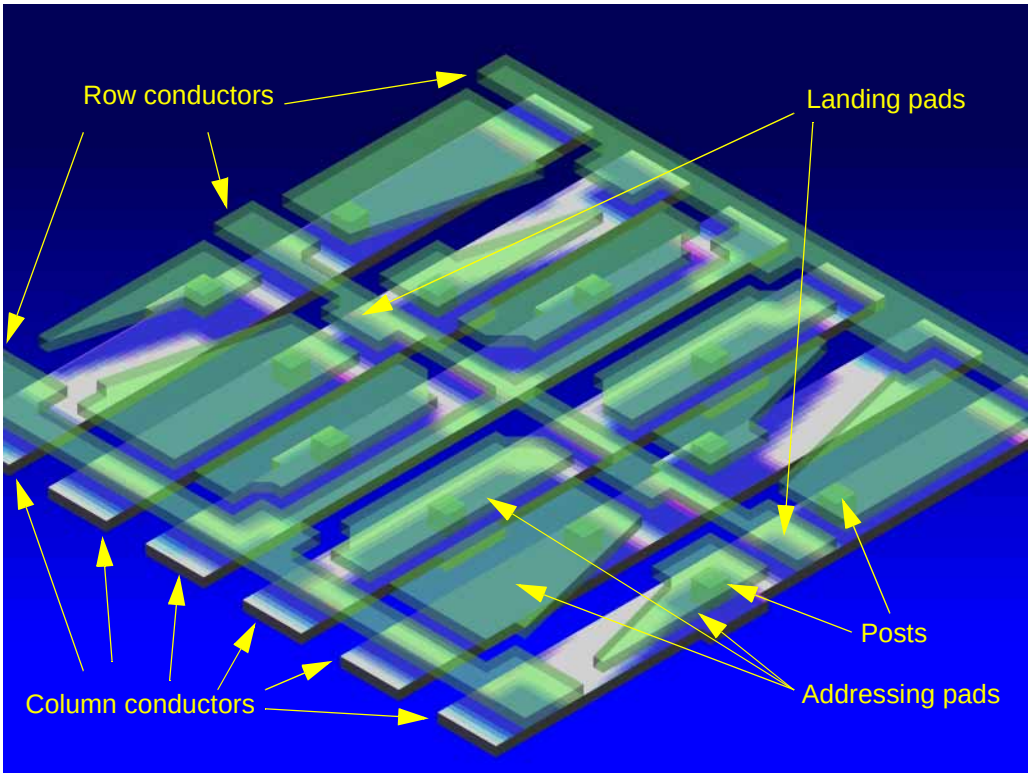


Figure 3.13 Pixel rendering showing the first two layers of polysilicon The bottom layer shows the column conductors. The top layer shows the addressing pads (odd shapes) and the row conductors and landing pads. Each addressing pad has a via or post down to the column conductors.

The topography of the spring layer in Figure 3.14 is not shown exactly, as these actually pass over the thicker yoke layer where they overlap. The position is correct as shown where they are not overlapping, and since the springs are extremely thin, this is a fairly accurate picture.

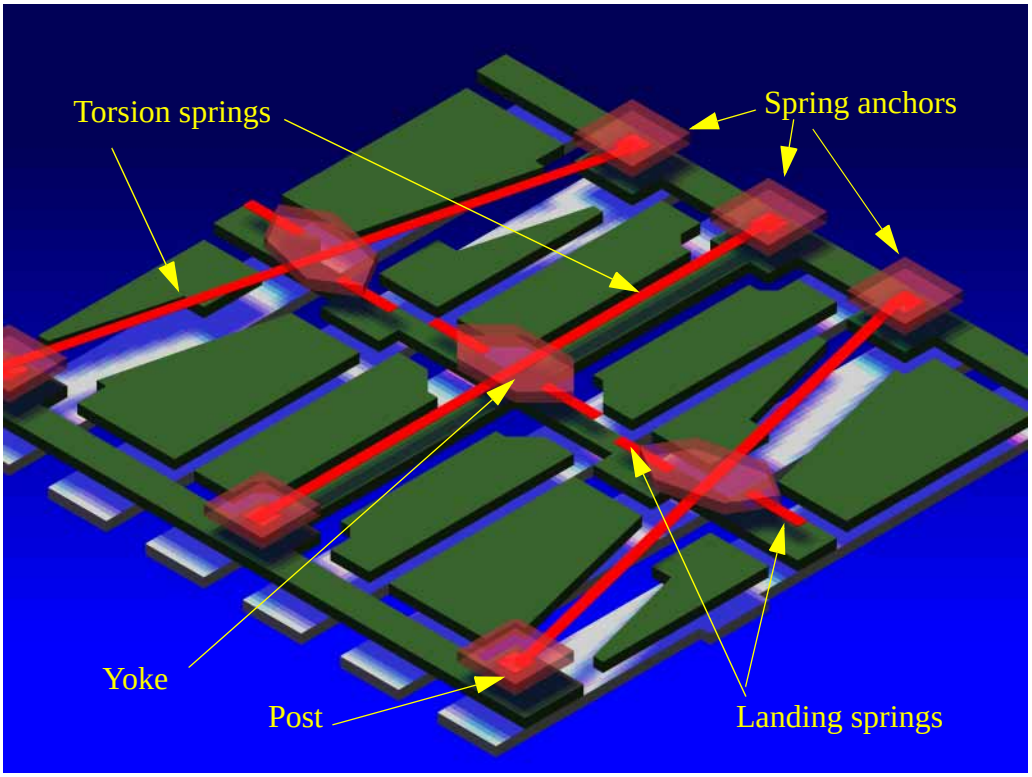


Figure 3.14 Pixel rendering showing the first four polysilicon layers.

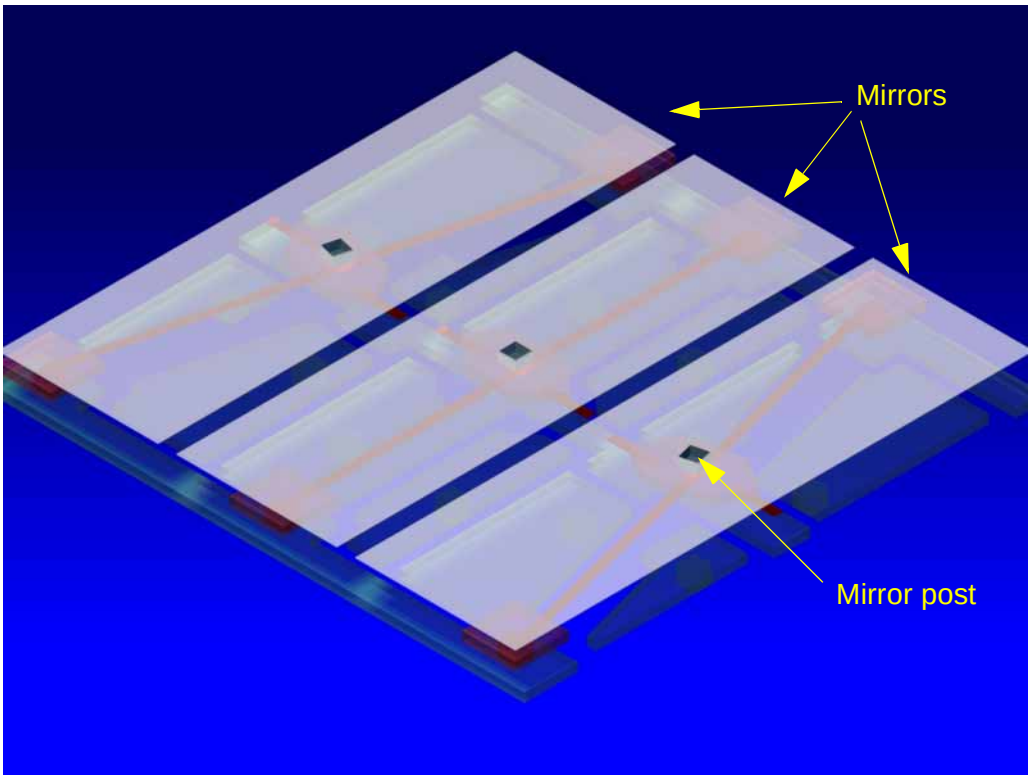


Figure 3.15 Pixel rendering showing top four polysilicon layers.

3.4 Sandia-Fabricated Designs

The Sandia National Laboratory offers a fabrication service to BSAC for their SUMMiT four-level polysilicon process. Eight small dies are combined with one die of test structures supplied by Sandia to form the mask set for a run. The space available requires a large number of projects. My project needs a quarter of one of the smaller dies. To map the micromirrors into the Sandia process, which cannot be changed, is the challenge.

My condensation of their many pages of designs rules is shown in Table 3.2.

Table 3.2 Summary of Sandia SUMMiT design rules

Mask Names	Minimum Size	Maximum Size	Minimum Space	Maximum Space	Nitride Cut	MMPoly0	Dimple1 Cut	SacOx1 Cut	MMPoly1	MMPoly1 Cut	Pin Joint Cut	SacOx2	SacOx2 Cut	MMPoly2	MMPoly2 Cut	Dimple3 Cut	SacOx3 Cut	MMPoly3	MMPoly3 Cut
Nitride Cut	1	4	1			A[a]													
MMPoly0	1		1		1			0.5	A					A				A	
Dimple1 Cut	1		1	50					R[b]	N	N			R[b]	N				
SacOx1 Cut	2		1						R[b]	N	N			R[b]	N				
MMPoly1	1		1				1[c]	1									1		
MMPoly1 Cut	1		1				-1	-1											
Pin Joint Cut	3		1					-1		N	-7[d]	R		R	N				
SacOx2	1		2								1								
SacOx2 Cut	2		1								-1	R							
MMPoly2	1		1				0.5	1,A		-0.5	A4						1		
MMPoly2 Cut	1		1	A38										R					
Dimple3 Cut	1.5		2											A	-A			R	N
SacOx3 Cut	2		2					0.5						A				R	N
MMPoly3	1		1														1 S[e]		
MMPoly3 Cut	1		1	A38															

a. A = advised -A = not advised R = required N = not permitted
b. Requires either MMPoly1 or MMPoly2
c. Numbers: + must enclose above by this distance. - must be spaced from by this distance
d. For rotation of hubs made with pinjoint cuts. Advisory.
e. S = some required for contact

The full description of the SUMMiT process is given in Appendix D.

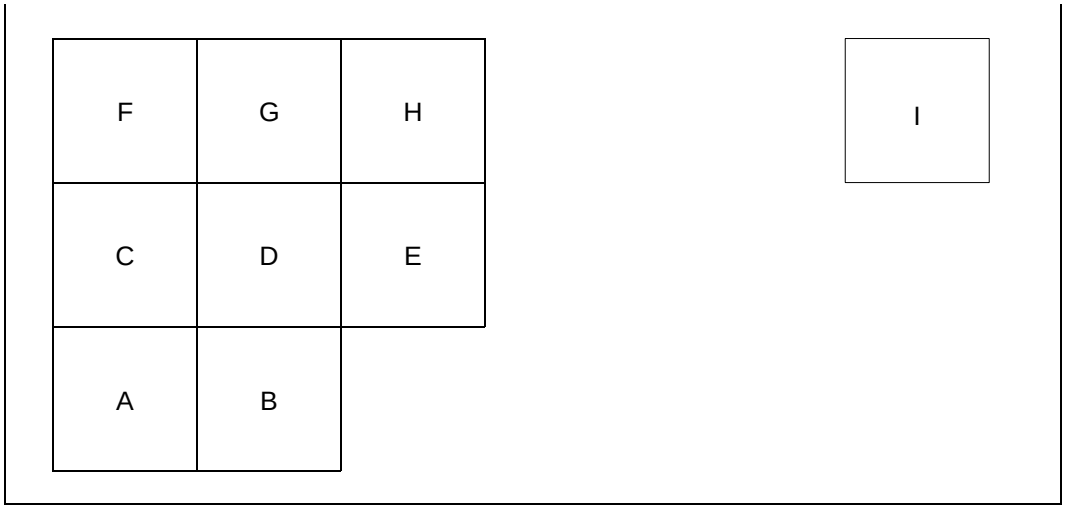
The main difficulty in mapping these micromirrors into the Sandia process is the thickness of the layers. There is no layer thin enough to form the torsion springs as they were designed for the Berkeley fab. The springs need to be redesigned with a new shape that will allow them to be more flexible than the straight bar shape, or to be eliminated altogether. If the springs are made much more flexible, then they will sag. Therefore a way has to be found to keep the mirrors from flattening down against the addressing pads.

The quarter die is large enough for nine small arrays of different pixel designs. I present each one of them in Section 3.5 that follows with an image from the AutoCAD layout of one pixel, and a description of the features of that variant.

The layout must be submitted in AutoCAD R14. I did my preliminary work in a much smaller cad package (Key CAD Complete) that I have available at home. Its output data exchange files (DXF) moved smoothly into AutoCAD to run the design rule checker.

A “feature” of AutoCAD is that items on the various layers are drawn onto the screen in apparently random orders. When the borders of two or more features are coincident, the color (usually different for each layer) that is seen in the layout will not be consistent. Specifically, just because one color appears to be on top of another in the figures, does not imply that the respective features are similarly on top of one another in the design.

Figure 3.16 shows the overall layout of the nine designs on the small die. Because one of the other students who shared the die had a strangely shaped object that needed to protrude into my section, we swapped a small amount of space, and my ninth design is situated well away from the others.



A. Horizontal serpentine spring
B. Ball bering and hinge in sloppy socket
C. Vertical serpentine spring - one micron gaps
D. Vertical serpentine spring - two micron gaps
E. Ball Bearing and hinge in tight socket
F. Spiral Spring - no hinge
G. Spiral spring - with loose hinge - two micron gap
H. Spiral spring - with tight hinge - two micron gap
I. Hexagonal - with tight hinges

Figure 3.16 Overall layout of the nine designs on the small die

Sandia's key to the colors of the AutoCAD designs is given in Table 3.3. Due to the repeated use of the same colors, the drawings are difficult to understand. (I apologize to readers who are reading a black-and-white copy of this dissertation, as I have no key that makes these drawings readable.)

Table 3.3 Mask level names and colors in SUMMiT process

Mask Level	Code	Color	Purpose
21 Nitride_Cut [a]	NIC	Purple	Substrate contacts
22 MMPoly0	P0	Magenta	Ground plane
23 Dimple1_Cut	D1C	Dk Blue	Dimples in P1
24 SacOx1_Cut	X1C	Green	Anchor P1
25 MMPoly1_Cut	P1C	Black	Holes in P1, no flange
26 Pin_Joint_Cut	PJC	Yellow	Holes in P1 w/flange
27 SacOx2	X2	Tan	Separate P1 & P2
28 MMPoly2	P2	Red	Define shapes in P2 and/or P1+P2
29 Dimple3_Cut	D3C	Yellow	Dimples in P3
30 SacOx3_Cut	X3C	Black	Anchor P3
31 MMPoly3	P3	Blue	Define shapes in P3
36 MMPoly1[b]	P1	Black	Defines shapes in P1
37 SacOx2_Cut [b]	X2C	Tan	Defines hole in X2
38 MMPoly2_Cut [b]	P2C	Red	Defines holes in P2
41 MMPoly3_Cut [b]	P3C	Blue	Defines holes in P3

a. Masks with "_Cut" in the name are dark-field masks (closed polygons define holes to be etched in film); others are light-field (closed polygons define structures in film to be left after etch)

b. These "drawing-only" layers are XORed with their master layers to form the mask (i.e., P1C xor P1 = P1C, X2 xor X2C = X2, P2 xor P2C = P2, P3 xor P3C = P3). Shapes in drawing layers are only valid inside shapes in the corresponding master layer!

The solution to the sagging springs is found in the dimples that are provided under the poly-3 layer to reduce sliding friction. These dimples are deposited in holes that are plasma etched into the sacrificial oxide layer, and so they form small cylinders or pins. I use these not for sliding, but to be pivot points. One of these can be seen in the cross-section drawing shown in Figure 3.17. The pivots must be pulled down into place (against the small restorative force of the spring) by a small bias voltage. In my designs, these poly-3

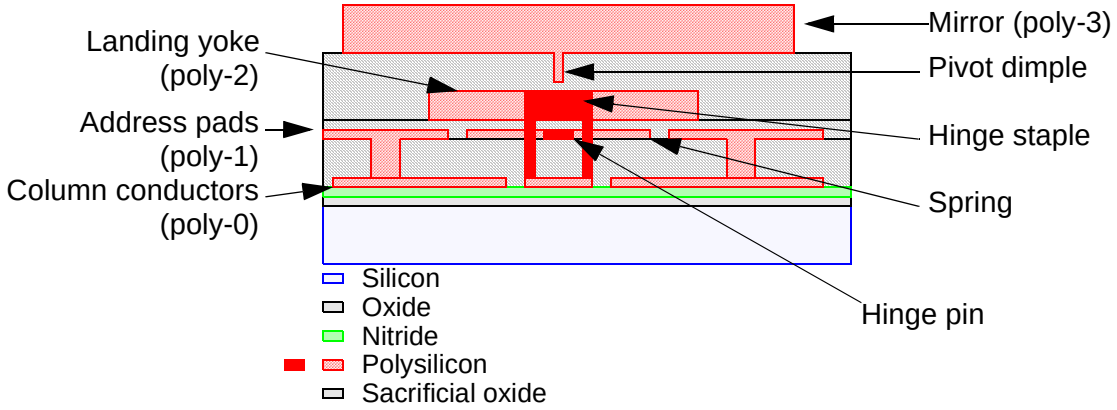


Figure 3.17 General cross-section drawing for micromirror devices implemented in the Sandia SUMMiT process

pins sit in small depressions in the poly-2 layer formed where poly-2 is joined to poly-1; the intention is that the depressions will help keep the pins from sliding sideways. Other noteworthy features that can be seen in the cross-section are: the hinge pin-and-staple used in some of the designs; the landing yoke that stops the rotation when the mirror touches down against it; and the spring that is fabricated from the 1.0μm thick poly-1 layer. The poly-0 layer is thinner, and so would make better springs, but it cannot be released for motion in this process.

Since I had no control over the thickness of the layers in this process, the 10° tilt for the mirrors is the major factor in sizing the features of the design. If the mirrors are made too large they won't be able to tilt far enough, and if they are too small the tilt angle will be too great.

Metallization. To increase the final reflectivity of the mirrors, all of these are designed to allow post-release metallization by evaporation (or perhaps even sputtering!) The largest concern about metallization would be shorting out conductors that are exposed either between mirrors in the array, or completely outside the array. Conductors on the poly-1 level and higher are not a problem because they are up off of the underlying layers: while they may get metallized in spots, they will not short to anything. The gaps between poly-0

conductors are very carefully hidden beneath the overhangs of higher level structures. The area surrounding the pixel array and the bonding pads has been covered with an all-inclusive "carport" structure that keeps the poly-0 conductors out of the "rain" of metal particles. This cover should also reduce stray light diffraction from the poly-0 layer and thereby increase contrast. The layout of these pixels overlaps with the next row due to the row conductor — notice, in Figure 3.18, the wide notch at the top edge of the poly-1 layer and the corresponding bulge at the bottom edge. This little detour serves to protect the column conductors from the metal. For the designs without springs, it may be necessary to "float" the mirrors to prevent "painting" them into whichever position they are in during metallization. Methods for floating could include ultrasonic agitation, or charging both mirrors and address pads to get some repulsive forces working to balance the mirror positions.

3.5 The Nine Designs

I present three groups of designs: serpentine springs ("A," "C" & "D"); spiral springs ("F," "G" & "H"); and hinged designs ("B," "E" & "I").

Figure 3.18 shows the layout for the first serpentine spring design (design "A"). The design differs from my earlier designs in several ways: each mirror is connected to its two springs near the ends of the mirror rather than in the center; the yokes that stop the mirror motion at 10° are at the ends of the mirrors and are stationary — the mirror stops against the yoke rather than the yoke stopping against a landing pad; and bias conductors on the poly-0 layer electrically connect the yokes to the mirrors and the row conductors.

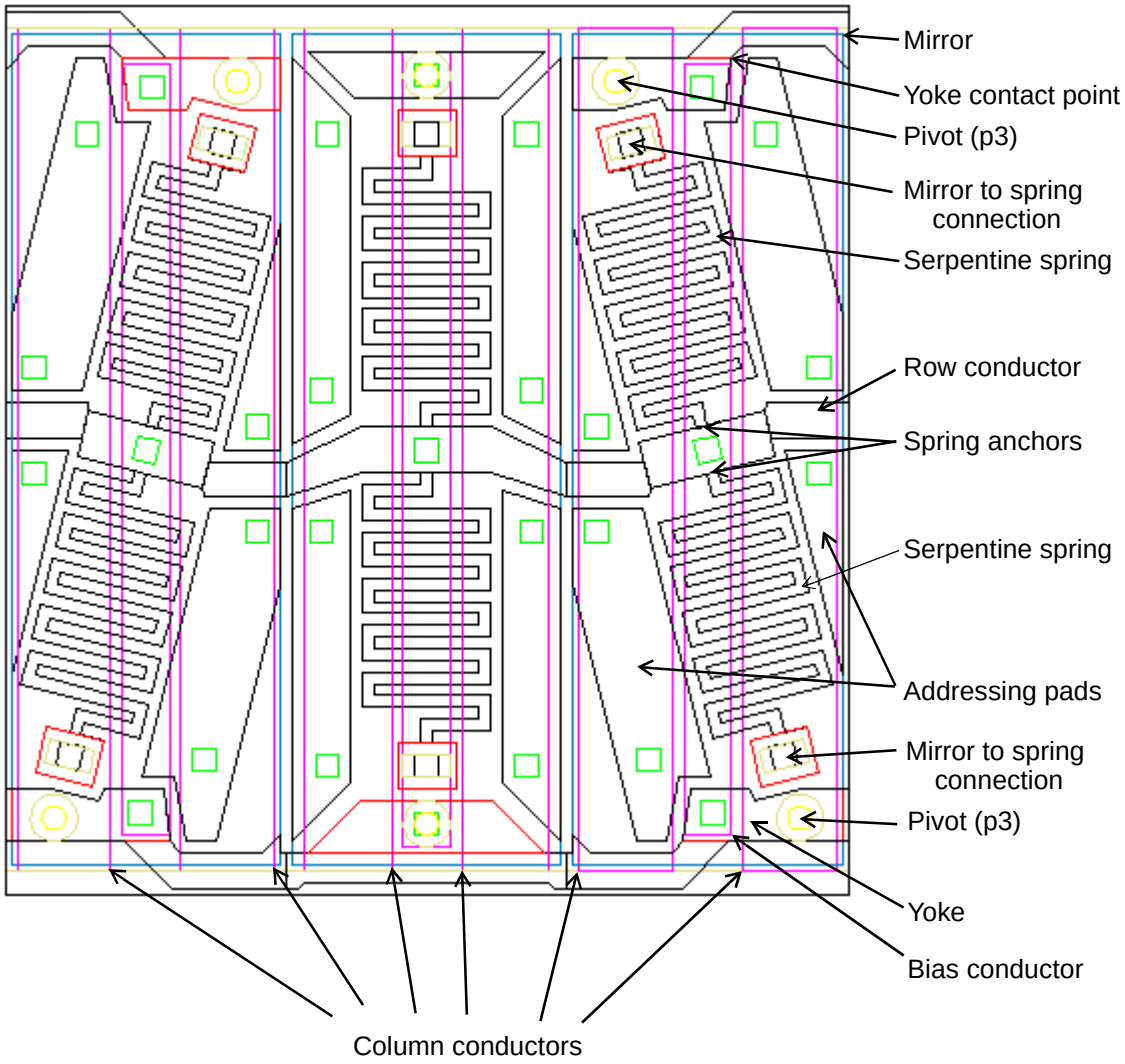


Figure 3.18 Serpentine springs — Design “A”

A method for further softening the springs, while keeping their area nearly constant is shown in Figure 3.19. The serpentine direction of the springs is changed from back-and-forth across the width of the mirror to following the length of the mirror. An easy way to think about the net torsional spring constant of these springs is to combine the six lengths of spring material into one long length. This results in a spring that is six times softer than a single-length spring. There is some bending in the short legs that connect the long ones, but that just softens the springs a little more.

In both the “C” and “D” designs, the row conductor only runs the full width of the pixel on the bottom edge; all of the features in the center of the mirrors have been removed, simplifying the addressing pads. The only difference between “C” and “D” is that the mirrors on “D” are 1.0μm smaller in both x and y to decrease the chance that the mirrors will strike each other.

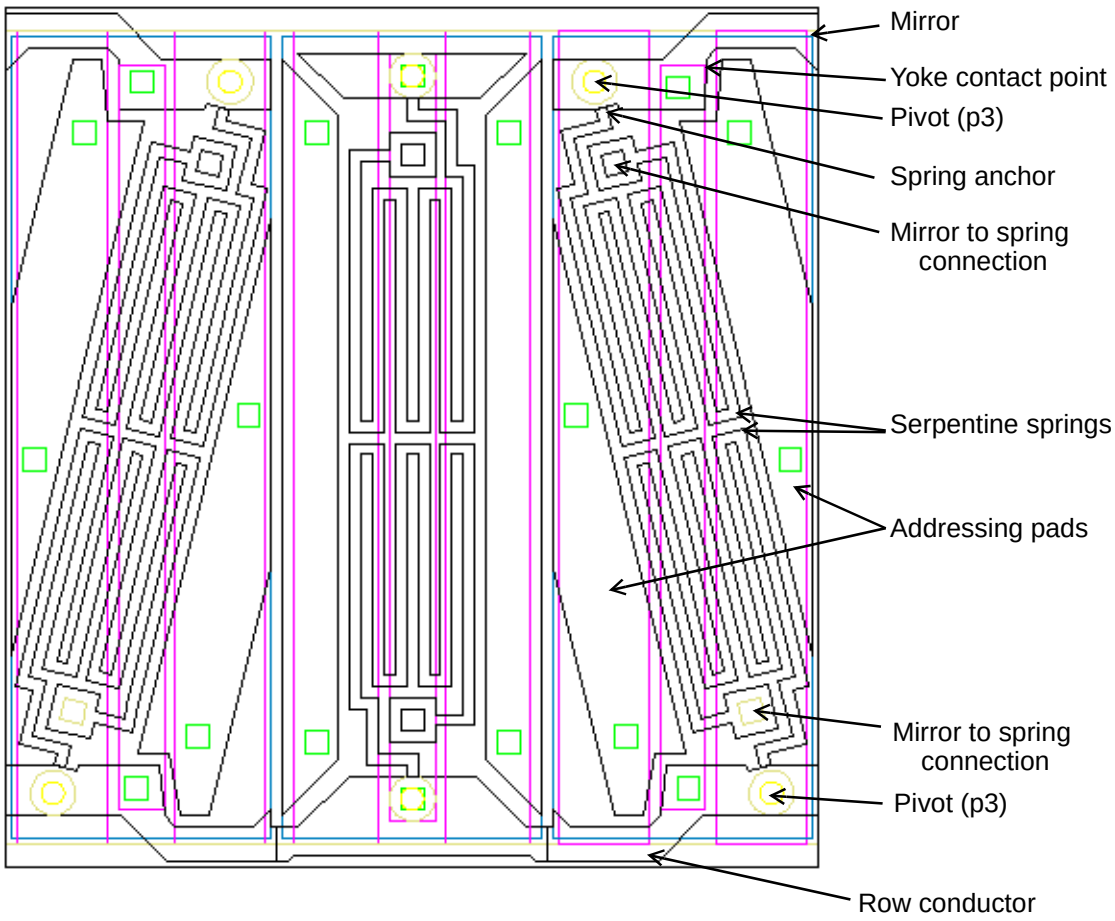


Figure 3.19 Length-wise serpentine spring layout — Designs “C” and “D”

The two springs acting in parallel in the “C” and “D” designs serve to increase the effective spring constant. The springs are connected in series for greater softening. The result (Figure 3.20) is a spiral spring with almost one-third of the stiffness.

The major concern with this design is that the entire mirror might become displaced laterally, as it is only fastened at one end. So why not fasten down the other end

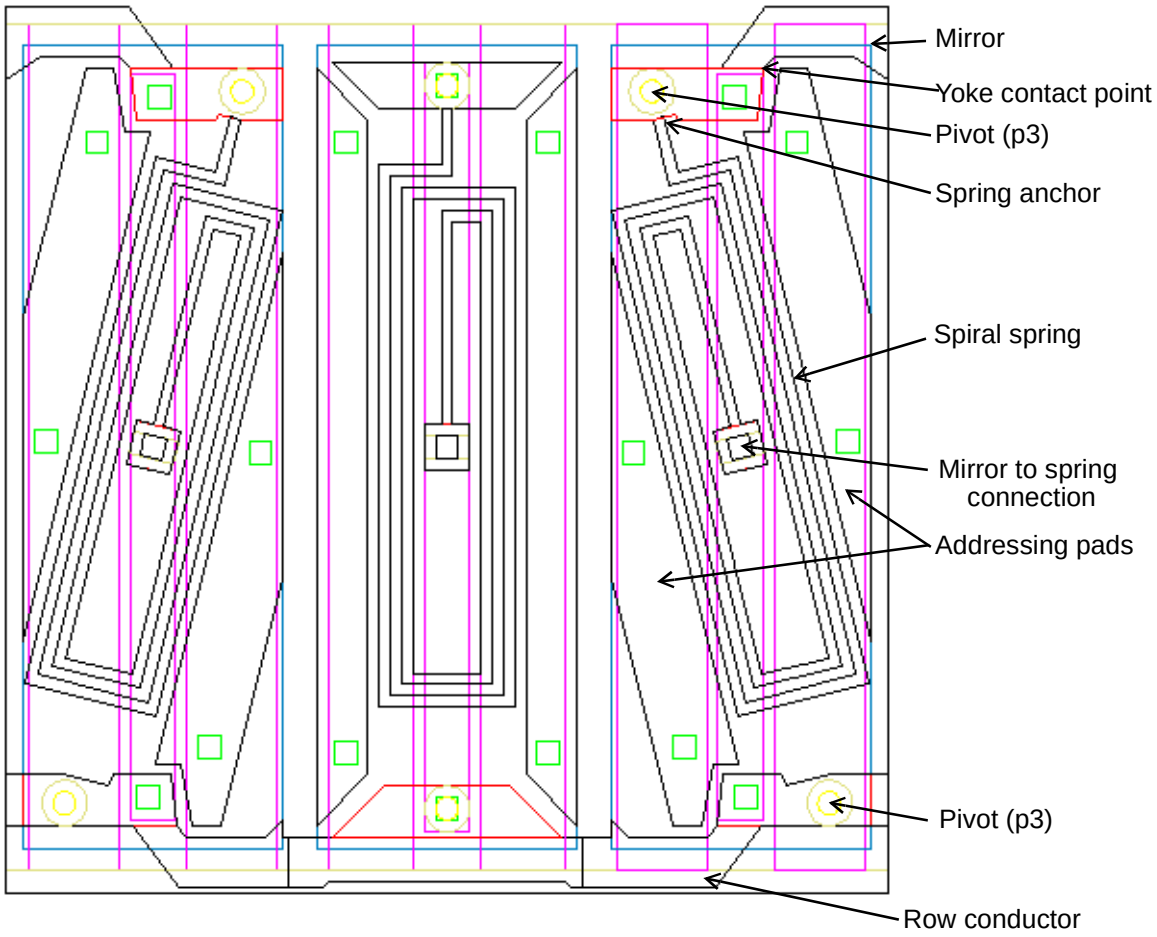


Figure 3.20 Spiral spring — Design “F”

somehow? The answer is Design “G” (Figure 3.21) where a pin-and-staple hinge with lithographically defined spacing is added to keep the mirror under better control.

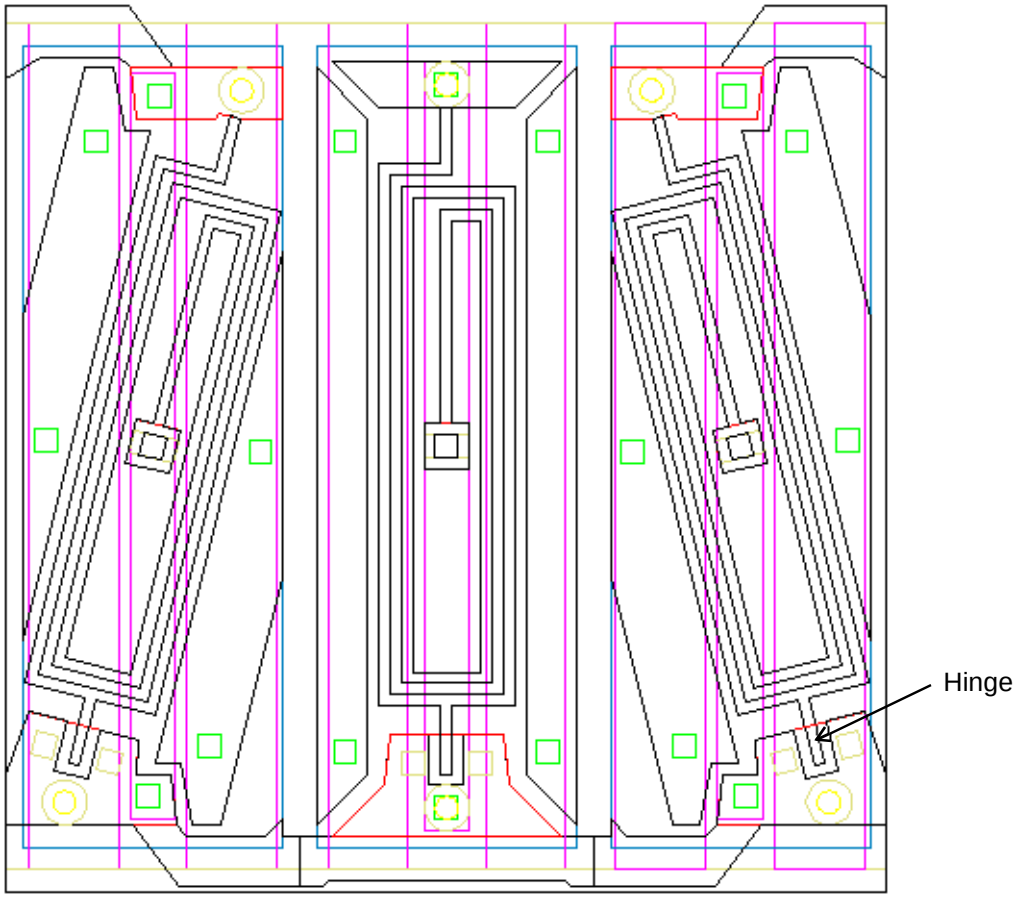


Figure 3.21 Spiral spring with hinge — Design “G”

To tighten the hinge tolerance, I use the mechanism that Sandia intended to produce tight-tolerance gear hubs. This new hinge, shown in Figure 3.22, uses the thin-film deposition thickness to control the spacing between poly-1 and poly-2; in this case, between the hinge pin and the surrounding socket. Design “H,” shown in Figure 3.23, uses this new hinge.

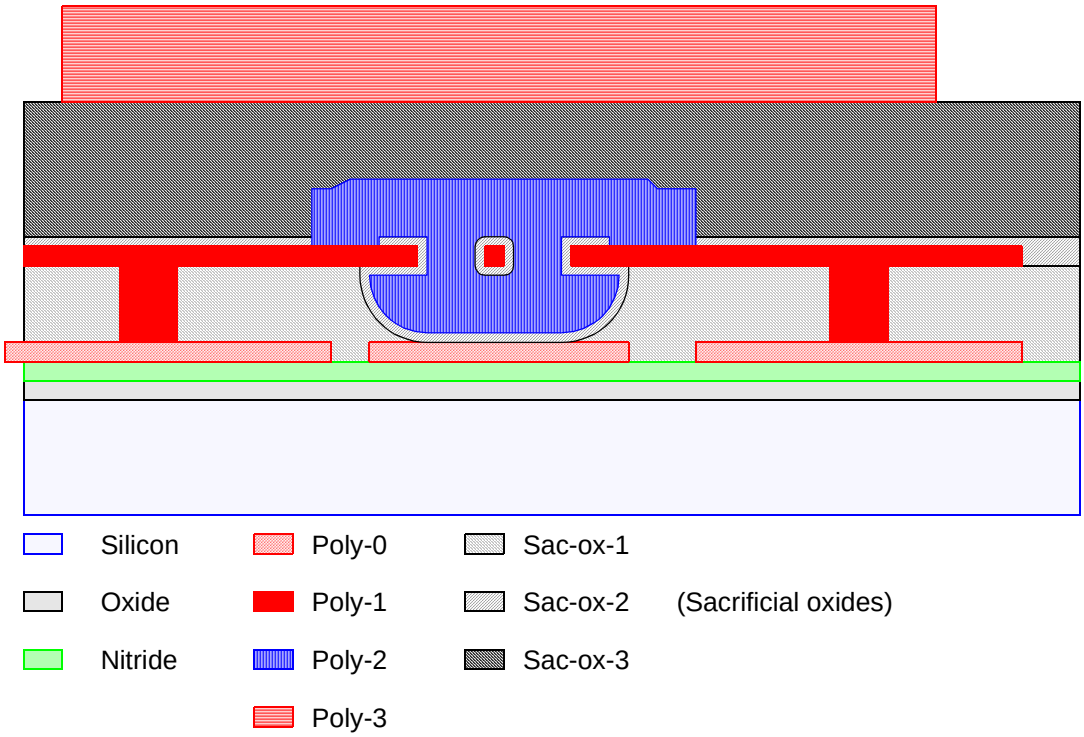


Figure 3.22 Cross-section drawing of a tight-tolerance hinge implemented in the Sandia SUMMiT process

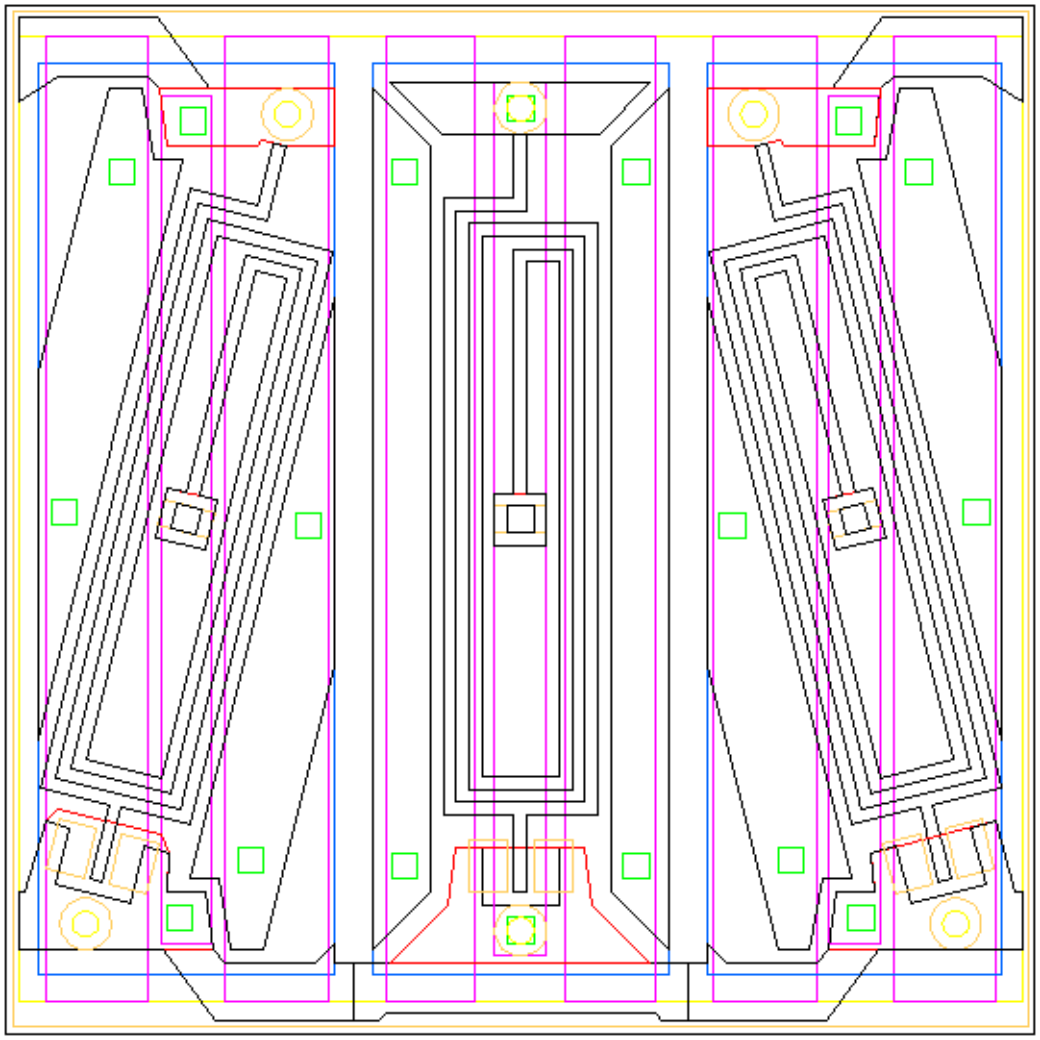


Figure 3.23 Tight-tolerance hinge — Design “H”

The tight-tolerance hinges brings us to a design with hinges only — no springs at all. The idea here is to use electrostatic force, acting solely on the edge of the mirror that is currently up, to overcome the stiction forces and tilt the mirror to the opposite angle. The disadvantage of this is that the column addressing voltages need to be much larger, and that there can be no bias voltage on the mirror while we move it, because it would simply keep the mirror locked down. A design with the new tight hinge is shown in Figure 3.24. This design also features a side-to-side overlap to accommodate a shared post between

adjacent pixels. The hinge in this and the next two designs, must pass a small current to charge the mirror; therefore the hinge must not be allowed to form a thick native oxide film. These devices should be stored and operated in an inert gas such as nitrogen or argon or in a very good vacuum.

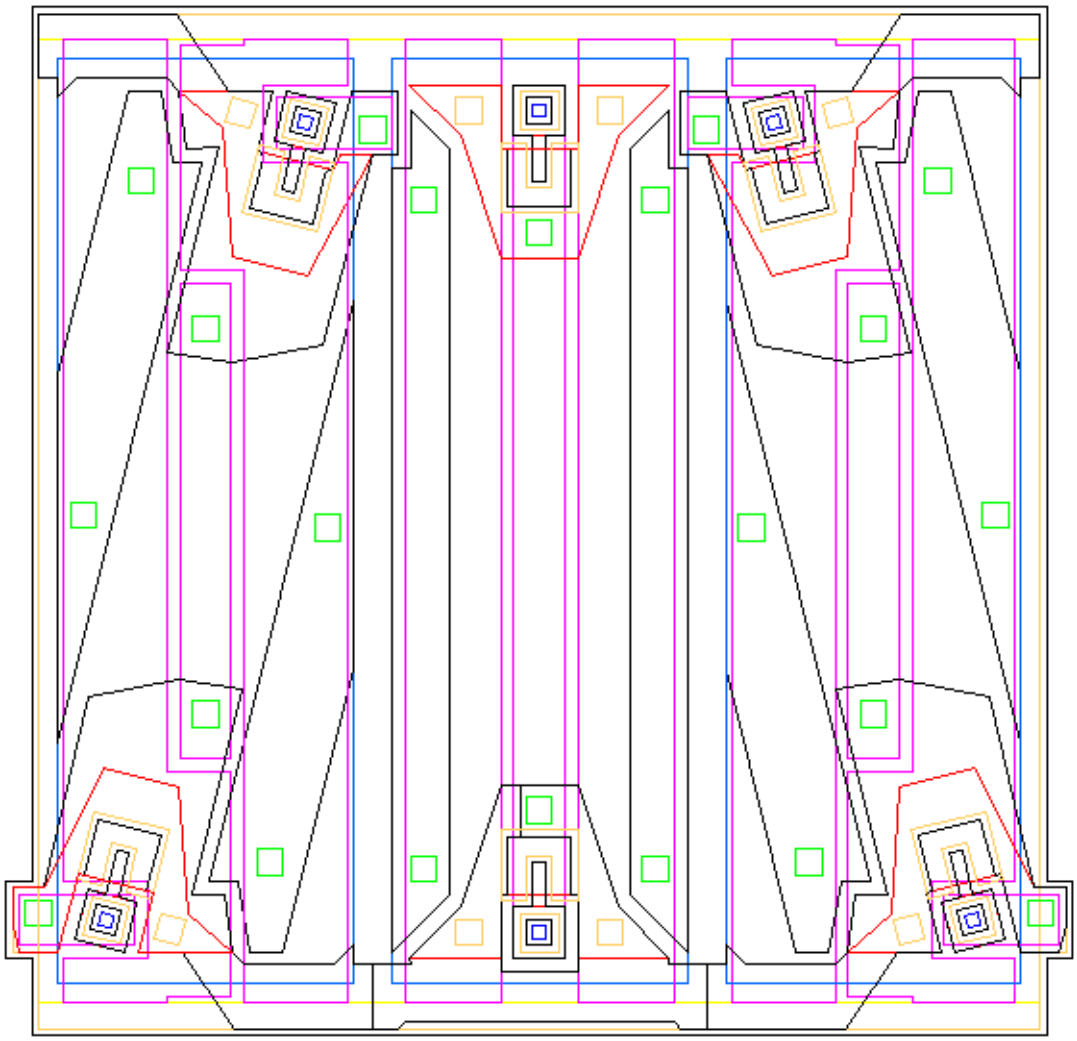


Figure 3.24 Tight-tolerance hinged mirror — Design “E”

Just in case the tight-tolerance hinge didn’t work as expected, a simple hinge unit was included as Design “B,” shown in Figure 3.25.

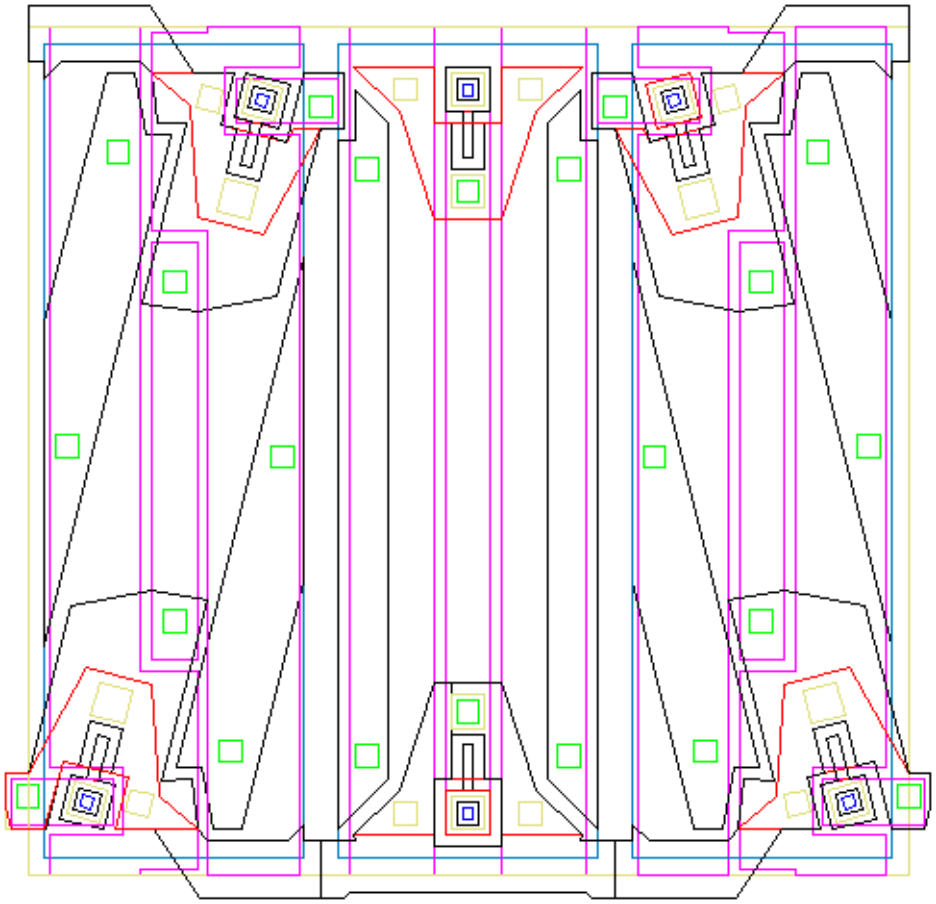


Figure 3.25 A simple hinged mirror — Design “B”

Since a hinged mirror doesn’t require all of the area for springs, the last design (Design “I”) on the die goes back to the hexagonal concept described at the beginning of this chapter. A new use for the poly-1 dimples, which are round as they are deposited in holes that are wet-etched, is to act as a “ball-bearing” pivot for the mirrors to rock on. The layout is shown in Figure 3.26 and a pseudo-3D image is shown in Figure 3.27.

We will describe the fabrication of the earlier designs in the Berkeley Microlab in the next chapter.

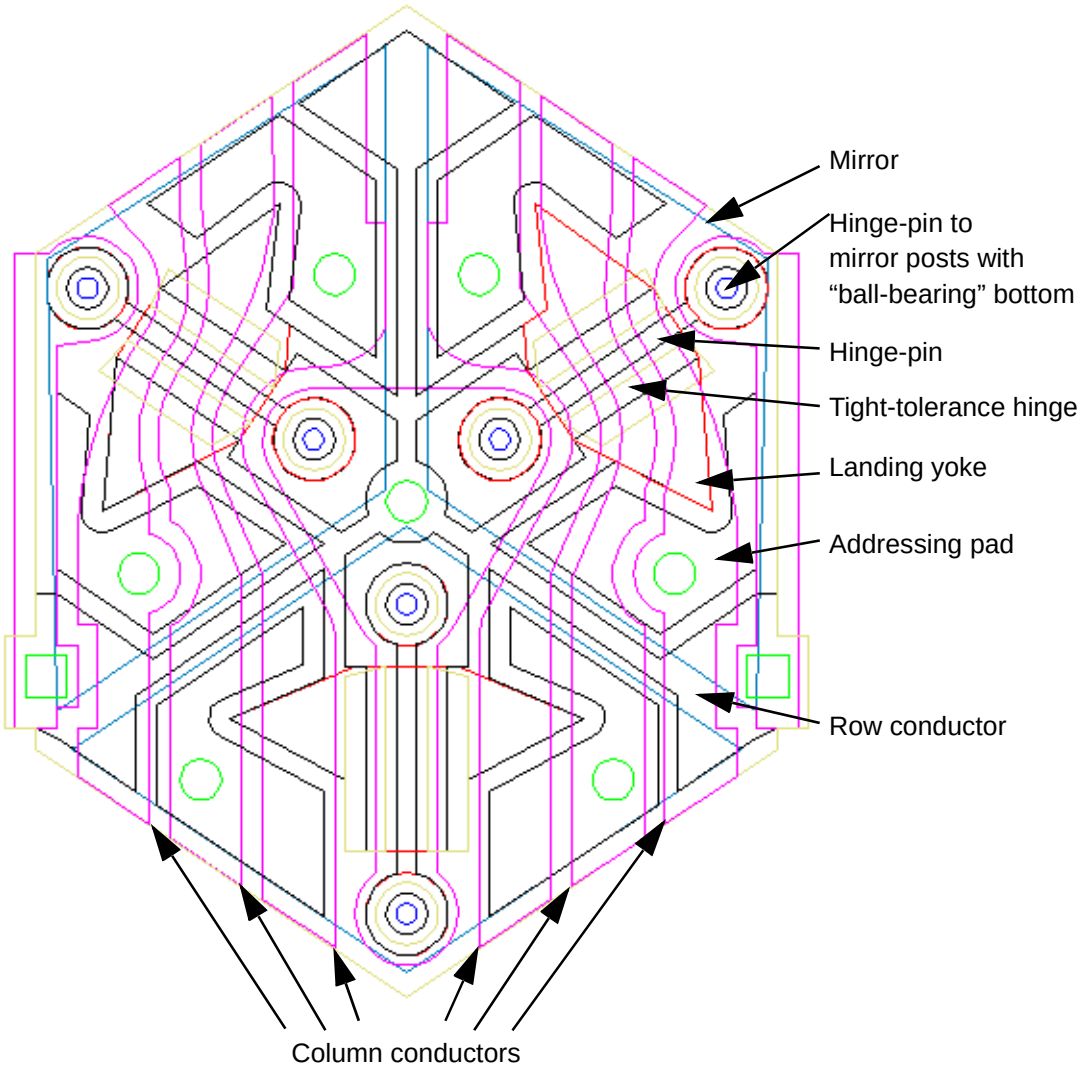


Figure 3.26 Hexagon pixel with tight-tolerance hinges — Design “I”

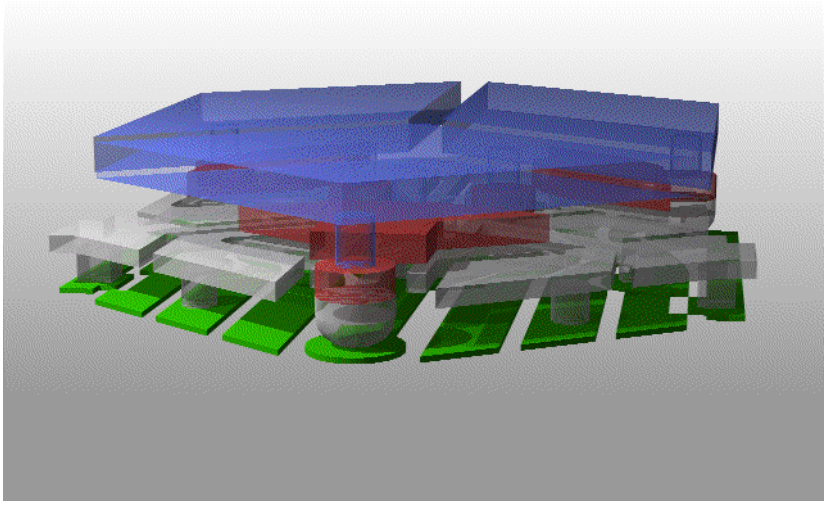
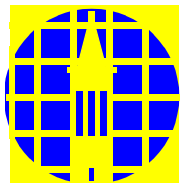


Figure 3.27 AutoCAD rendering of hexagonal-pixel hinged-mirror — Design “I”

4. Fabrication at Berkeley



The U.C. Berkeley Microfabrication Laboratory provides a capability, unmatched in academia, to researchers to fabricate novel structures. It may not be the largest cleanroom, or have the newest equipment, but it has a large number of users and an amazing staff that keeps the hundreds of pieces of equipment running and the storerooms well stocked with whatever supplies might be needed.

The lab is set up primarily to process 100mm (4-inch) wafers, including the pre-furnace wet-sinks used to ultra-clean wafers. These sinks accommodate small cassettes that hold 12 wafers. Since many processes require the inclusion of one or two test wafers along with those being processed, I used a lot size of 10 wafers. The finished devices tested in the next chapter are part of my eighth lot of wafers. Each of the prior lots had a processing error that provided a learning experience and encouraged more careful or skill-ful work on the next lot.

4.1 Basic Process

In this description, I present the basic fabrication process, omitting the myriad details that are included in Appendix A. As I describe the process used to fabricate the micromirror devices, I will present cross-section drawings of the center mirror, which steers green light. These cross-sections are somewhat unusual for MEMS because they are to scale in the vertical axis. This is only possible because of the extremely small size of the mirrors. Please note that these cross-sections have no “depth,” that is, objects that are not in the plane of the section do not appear in the figures. Where it is appropriate I will show different cross sections, A-A, through D-D, as defined in Figure 4.1.

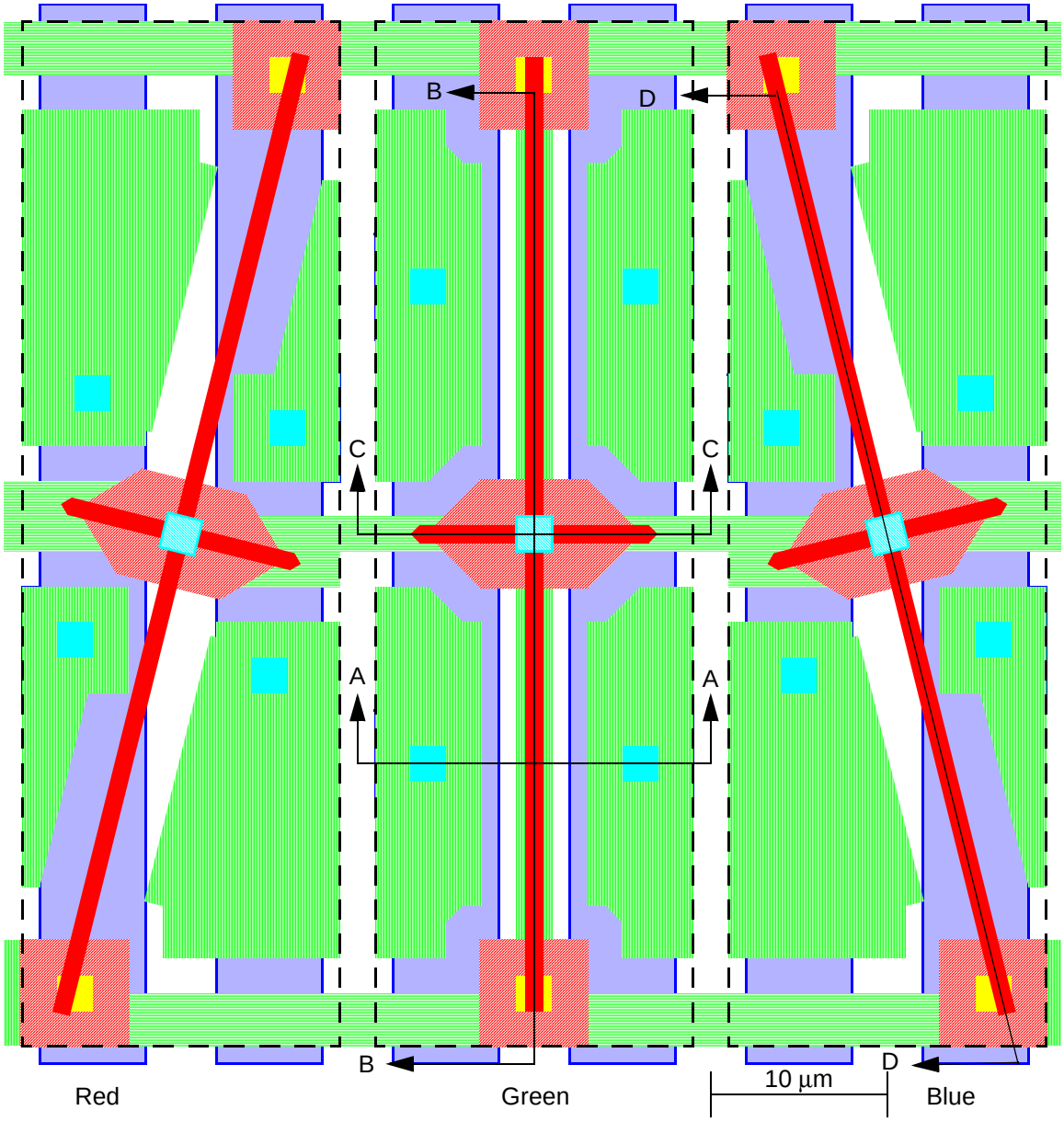


Figure 4.1 Cross-section definitions
(See Figure 3.5 on page 33 for key to the colors and patterns.)

These process steps can be broken into major groups. Steps 1 to 5 create the column conductors and provide a foundation for the addressing pads and row conductors formed in Steps 6 through 9. The yokes, springs and supports are formed in Steps 10 to 13, and Steps 14-17 complete the mirrors and release.

Figure 4.2 presents the key to the materials used in these cross-section drawings.

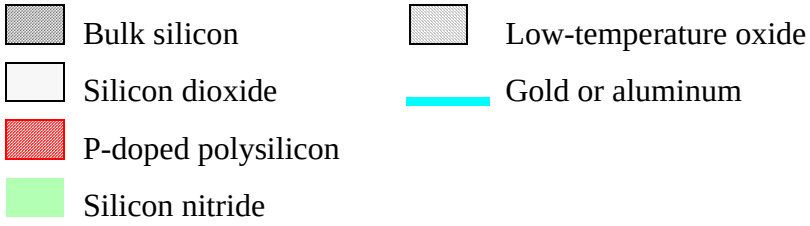
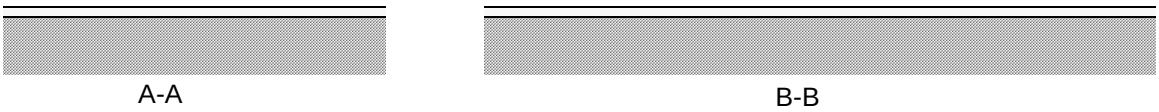


Figure 4.2 Materials key for the cross-section drawings.

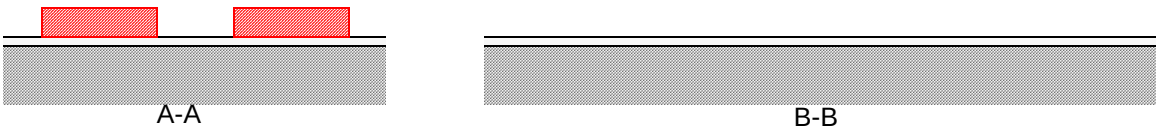
Step 1. Grow a base insulating layer of thermal oxide. This layer serves to insulate the column conductors from the bulk silicon. Its thickness controls the capacitance between those conductors and the bulk. This layer is not sacrificial.

Figure 4.3 Sections A-A and B-B after Step 1



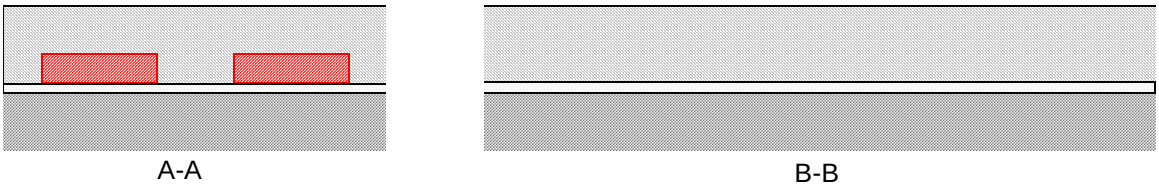
Step 2. Deposit and pattern doped polysilicon column conductors.

Figure 4.4 Sections after Step 2



Step 3. Deposit low-temperature oxide (LTO) and CMP flat.

Figure 4.5 Sections after Step 3



Step 4. Pattern the die edges. Each of the six sub-die clusters is surrounded by this moat that is larger than the saw cuts that will pass through them.

Figure 4.6 Moat pattern surrounding sub-die clusters and processing aids

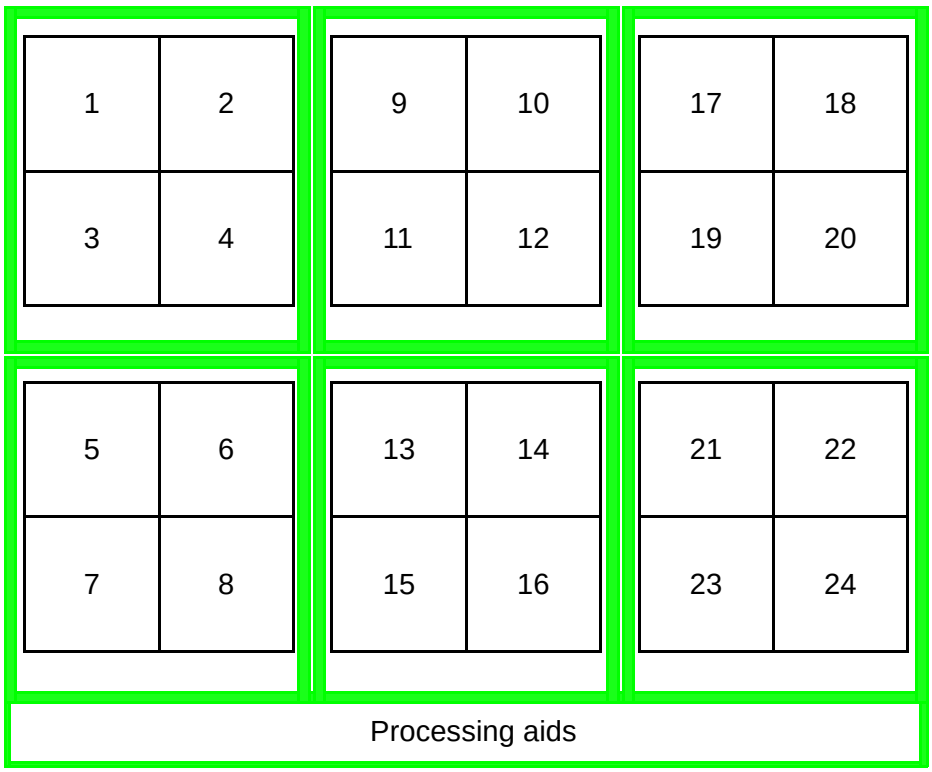
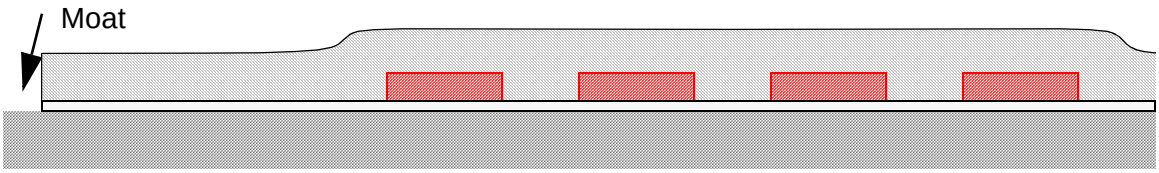
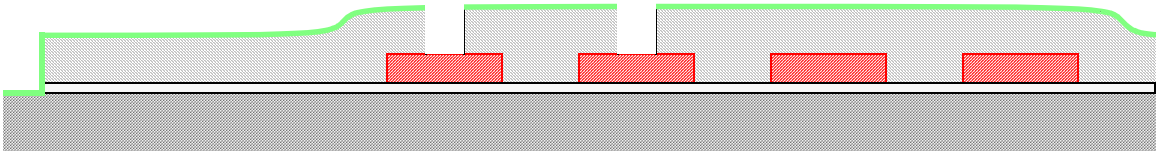


Figure 4.7 Simplified cross-section showing the edge of die after Step 4



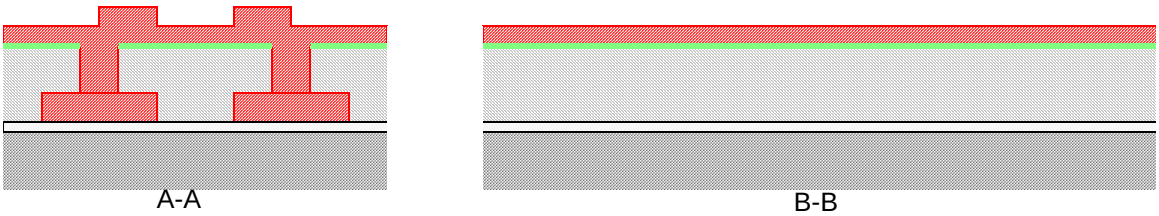
Step 5. Deposit silicon nitride and pattern contacts through the nitride and the LTO. The nitride layer protects the thermal oxide and LTO during the final release etch. This nitride coated oxide provides a solid base to the address pads on the next layer so that they will not flex during operation of the device.

Figure 4.8 Simplified cross-section showing nitride protection of a chip edge after Step 5



Step 6. Deposit and pattern thick addressing polysilicon. This step uses a timed etch in order to leave a residual layer of poly to be patterned later. The idea behind creating two level address pads is to increase the attractive electrostatic forces near the center of the mirrors so that lower bias voltages can be used. The mask for this step only implements this idea on some of the sub-die. This mask step is not currently used at all because it makes the planarizing much more difficult.

Figure 4.9 Cross-sections after Step 6

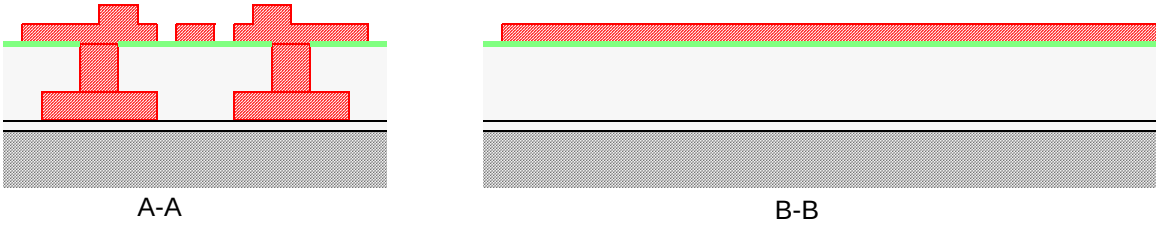


There is another step that is intended to place silicon nitride “bumpers” on the corners of the raised extra-thick poly address pads to prevent the mirrors from bending too close to the pads, shorting the drive voltages and welding themselves down. This step was omitted in the early runs because the extra-thick poly was a separate deposition and the other nitride layer is exposed. In the later runs there was no need for the bumpers, as the thicker poly was not included. Such a nitride layer might cause long-term problems by becoming electrically charged.

Step 7. Pattern the polysilicon row conductors, landing pads and low electrodes. The high electrodes are illustrated here to show how they could work, but do not appear in sub-

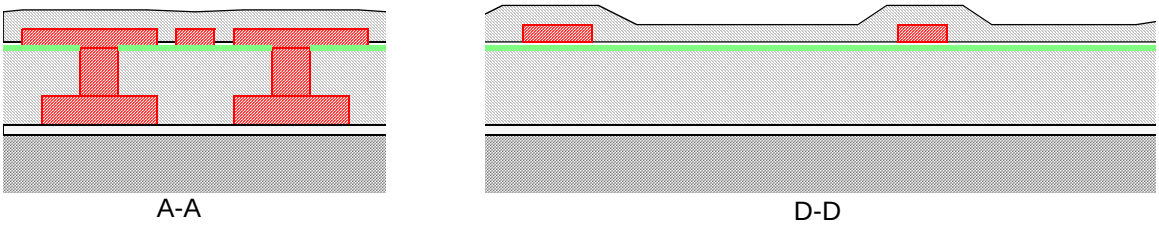
sequent drawings.

Figure 4.10 Cross-sections after Step 7



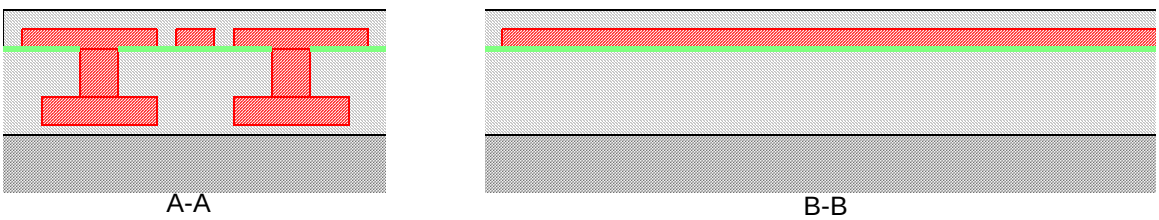
Step 8. Deposit LTO.

Figure 4.11 Cross-sections after Step 8



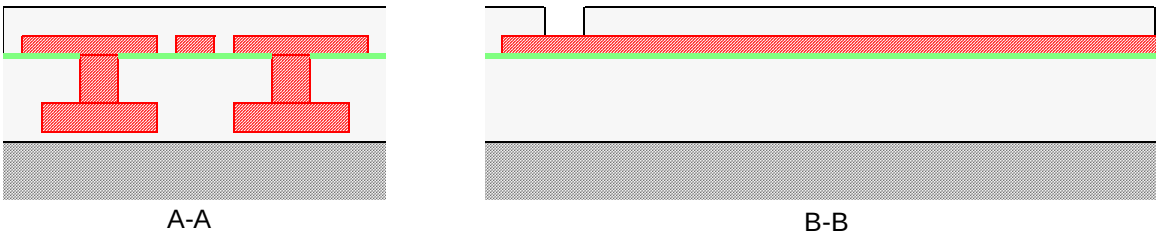
Step 9. Chemical-mechanical polish[75] (CMP) flat to expose the polysilicon structures; then redeposit LTO to the required spacing for the springs (z_{sp}). CMP is required to flatten the surface at this stage, so that the torsion springs can lie flat. CMP alone is far too non-uniform across a wafer to achieve the required thickness of LTO to support the springs. Polishing down to the poly in the center of the wafer, so that the sacrificial LTO layer thickness can be accurate, causes some loss of poly thickness near the edge of the wafer.

Figure 4.12 Cross-sections after Step 9



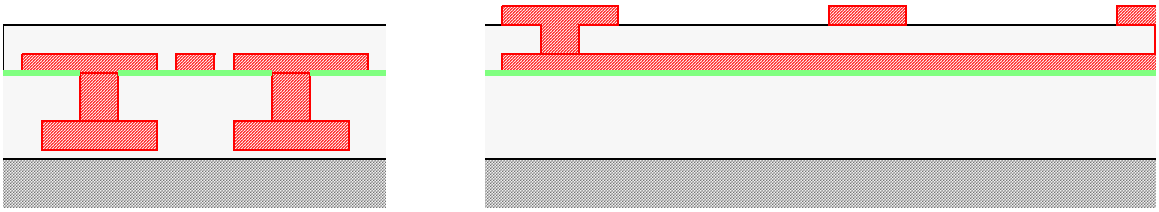
Step 10. Pattern the spring post holes.

Figure 4.13 Cross-sections after Step 10



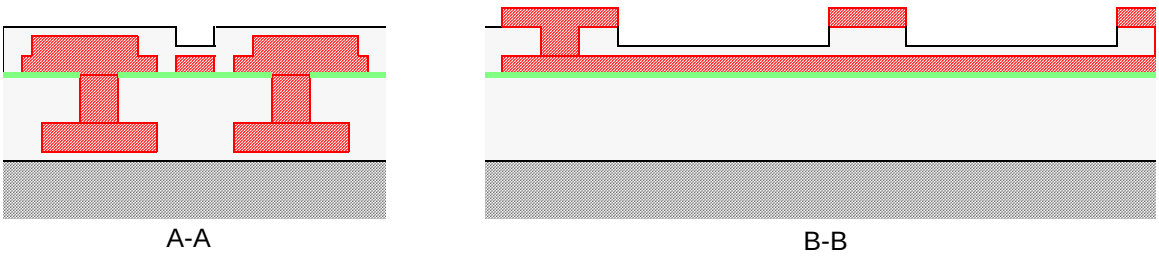
Step 11. Deposit and pattern spring posts and yoke polysilicon.

Figure 4.14 Cross-sections after Step 11



Step 12. Pattern trenches for the vertical “stringer” springs. Only one-quarter of the devices get this treatment. It is dangerous to skip this step, because if the stringers don’t form, then nothing will anchor the yokes and mirrors on these devices and the mirrors will float away during release and could contaminate the remaining devices. Unfortunately, there is a stringer-spring device on each of the smaller releasable areas of the chip.

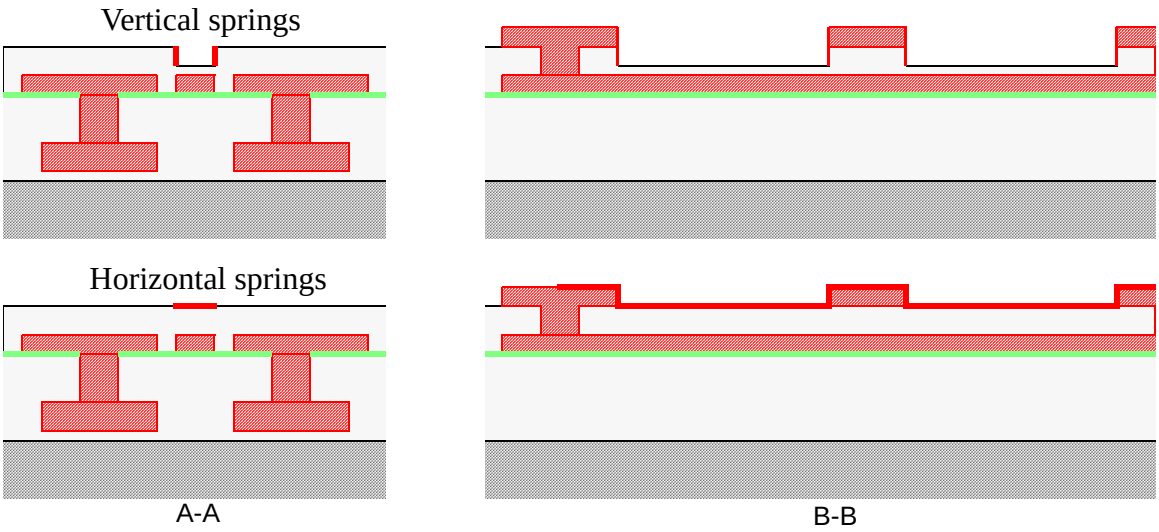
Figure 4.15 Cross-sections after Step 12



Step 13. Deposit and pattern ultra-thin-film springs of silicon. This step deposits doped amorphous silicon which is rapidly thermal annealed (RTA) to form tensile polysilicon

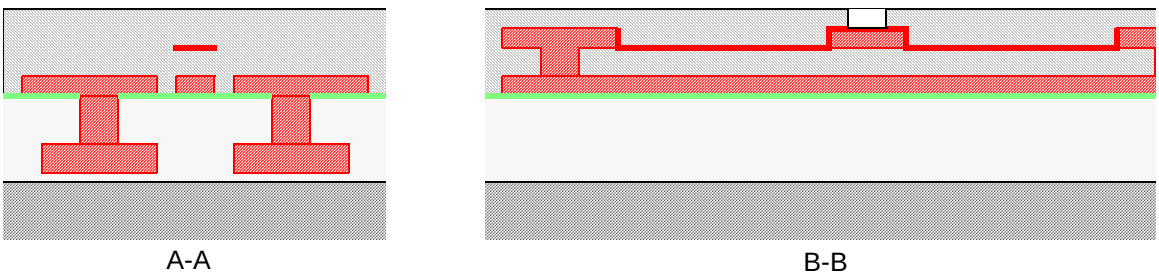
[76]. Note that no mask is required to form the stringers. Also note that the posts and yokes are not protected by photoresist during this etch; protection is not needed because the film is so thin and the coverage of yokes and posts is low enough that it is easy to obtain a strong end-point signal on the etcher.

Figure 4.16 Cross-sections after Step 13
for both vertical and horizontal springs



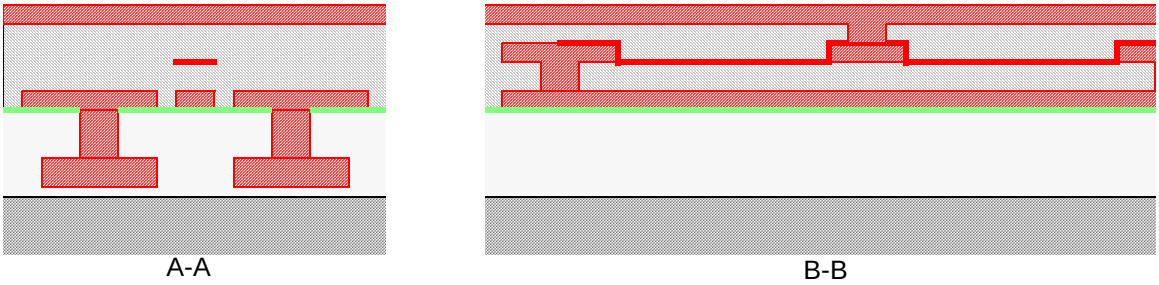
Step 14. Deposit LTO. CMP back to the posts and deposit and pattern more LTO. This CMP step is necessary to form flat mirrors. It was skipped in my test fabrications to save time and to eliminate the associated high risk. This layer completes the sacrificial material between the mirrors and the address pads.

Figure 4.17 Cross-sections after Step 14



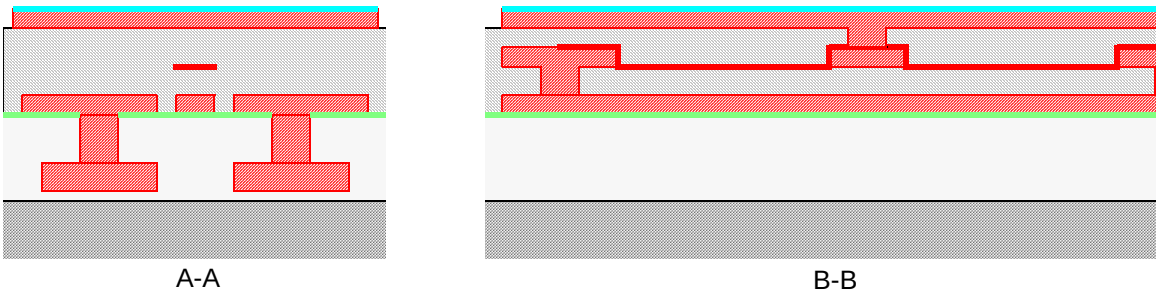
Step 15. Deposit polysilicon for mirrors and lightly CMP to achieve a mirror finish.

Figure 4.18 Cross-sections after Step 15



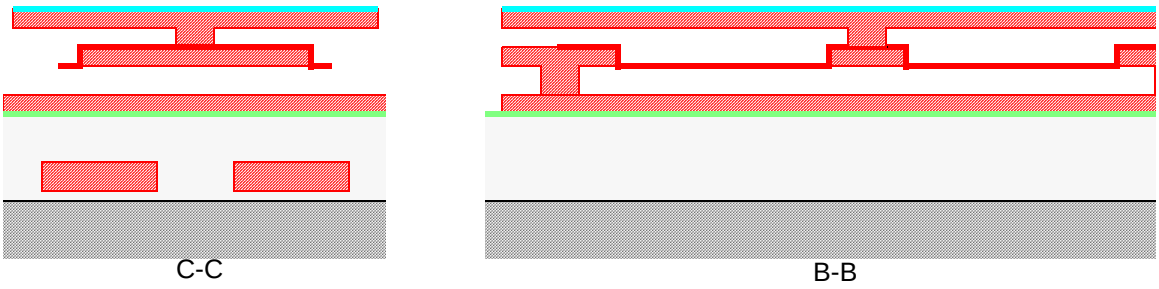
Step 16. Deposit gold reflective layer and pattern down through the poly mirrors. This step was skipped to save time.

Figure 4.19 Cross-sections after Step 16



Step 17. Saw wafers before sacrificial etch and critical point CO_2 dry.

Figure 4.20 Cross-sections after release



4.2 Processing Aids

Processing aids are gadgets that are designed into the mask set to help with the fabrication process. On these designs these include:

1. The very necessary alignment targets, used to align the wafers to the stepper in all but the first lithography step, that I include on every mask layer (see Figure 4.21);
2. Resolution patterns that allow gauging focus and exposure (see Figure 4.21);

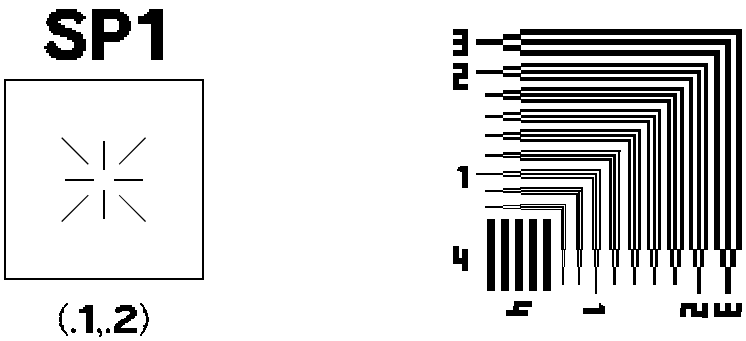


Figure 4.21 Alignment target and resolution elbows

3. Alignment verniers, patterns that show sub-micron alignment between layers;

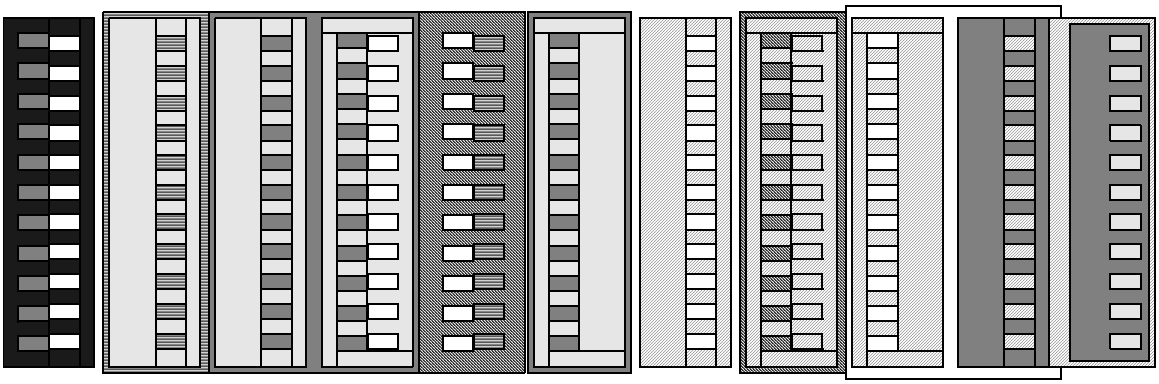


Figure 4.22 Alignment verniers

4. Test squares that are specifically set up to allow interferometric thickness measurements of deposited thin films;

5. "Dog bones" in poly-silicon layers that allow probing of resistance to confirm etch completion, layer-to-layer contact resistance, and film resistance; and

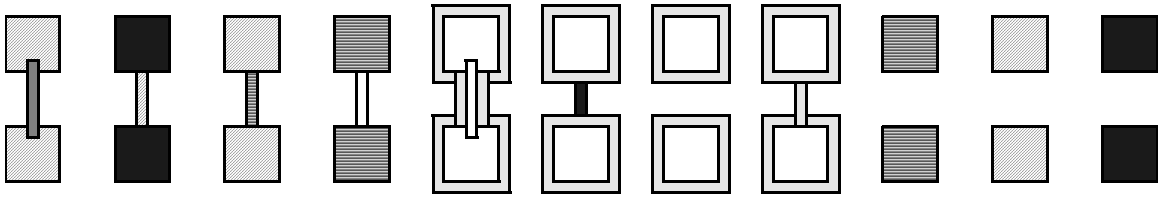


Figure 4.23 "Dog bones"

6. Strain gauges[77] that allow direct measurement of thin-film strain after release. A minor improvement to Liwei Lin's design for this gauge allows read-out of the angle from the vernier in tenths of degrees. Whole degrees are read on the stationary part where the center tine of the moving part points. Tenths are read on the moving part where the best match occurs. By curving the two scales, large motions may be accommodated.

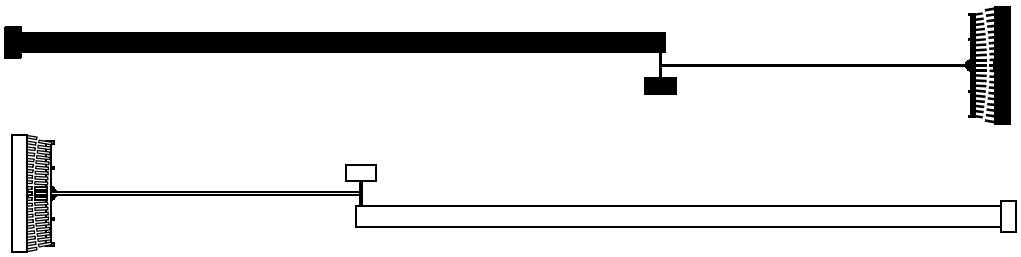


Figure 4.24 Strain gauges

4.3 Mistakes and Processing Advice

Here are a few of my mistakes and some advice on avoiding them.

1. High-temperature (over 900°C) anneals of LTO or PSG layers that are deposited over or under doped polysilicon or silicon-nitride layers may cause the formation of bubbles in the film known as “poly-pox.”

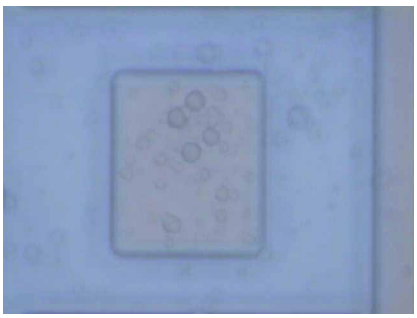


Figure 4.25 Poly pox.
The whole image is about 100 microns across.

2. When choosing between I-line and G-line resist for photolithography, be aware that I-line resist, despite its higher resolution capabilities, is more difficult to make work well, requiring longer exposures on the gcaws, and a precise post-exposure-bake.

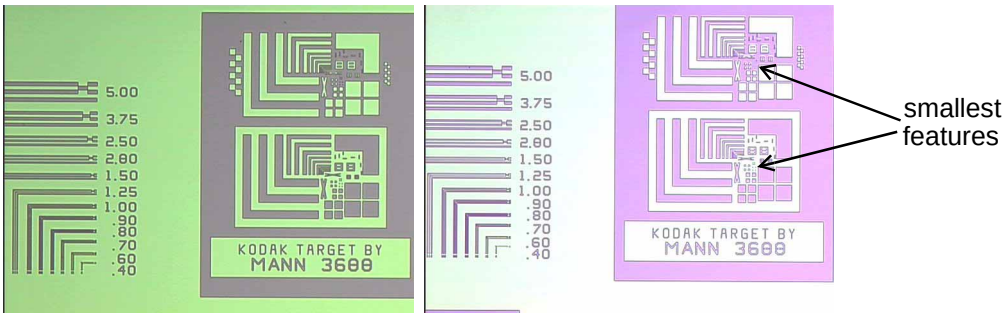


Figure 4.26 G-line and I-line test exposure patterns.
The tiniest features are missing from the positive version of the I-line in order to make the smallest holes in the emulsion.

3. Long etches in the oxide etcher cause the temperature of the wafer to rise, and turn the photoresist into an un-removable glop. Use the recipe “LONGSIO2” to break the etch up into short intervals and let the wafer cool down.

4. Trying to use end-point detection on the oxide etcher is a recipe for disaster. Most oxide etches do not have sufficient exposed area to use this feature. Use timed etches and be aware that tiny holes etch slower than large ones.
5. Don't skip the de-scum step in the photolithography module, especially on dark-field masks that make small contact holes in the resist.
6. When depositing amorphous silicon over polysilicon, you will find crystallites like the one shown in Figure 4.27. You may be able to contain these to contact structures by choosing which levels to make with each material.

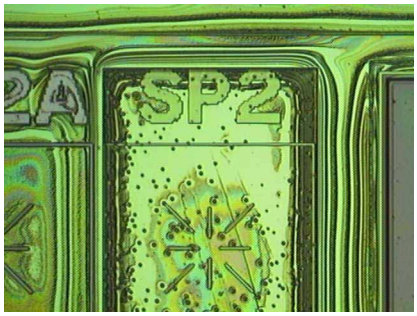


Figure 4.27 Crystallites

7. Too many mask layers in a process raise the risk of failure exponentially. Count on losing a wafer about every second mask. Think about ways to reduce the number of masks in your process.
8. Trying to do process characterization on wafers that you have a lot of time invested in is risky. It is far better to spend more time and do short test runs on test wafers.

9. Wet etching with only one coat of photo-resist can lead to unintended etching through pin-holes in the resist, as shown in Figure 4.28. This problem may be related to I-line resist.

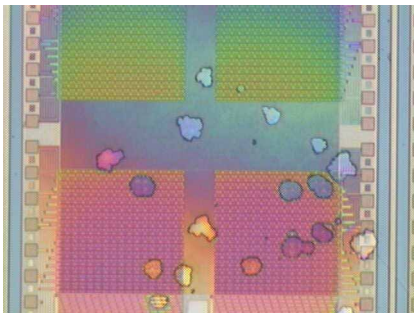


Figure 4.28 Unintended etching through pin-holes in a single layer of photoresist

5. Testing

There were three phases to my testing: tests that had to be run during the design phase to check feasibility; tests run during the fabrication process to develop process procedures; and, when the fabrication is complete, tests of device performance. The tests in the first two phases tend to be simple with only one or two lithography steps involved, although sometimes they need to be repeated to work out the details. I call these simple tests “short-loop” tests.

5.1 Short-Loop Tests

Testing of process ideas took place all through my fabrication cycle.

- An early test on torsion springs, fabricated out of 500Å thick polysilicon and supporting large flags designed to hang at approximately 45° when the chip is inverted, verified the spring constant equation and that structures could be made from such a thin film.
- A test run of sputtered aluminum mirrors deposited on a patterned sacrificial layer of photoresist and released in an oxygen plasma showed that we could duplicate the TI process if needed.
- An HF release of aluminized mirrors showed discoloration of the aluminum, leading to the creation of the post-release metallization designs incorporated into the Sandia run.
- A wet release and wet inspection of the on-chip strain gauges showed that doped polysilicon can be made tensile[76] for fabricating the torsion springs.
- A mirrors-only sample that was pulled straight to air from an HF release-etch had a large number of mirrors stuck down to the substrate, which indicated the need for a drying step.

- An HF release and CO_2 dry of a mirrors-only sample showed that very slow fluid flows are required to avoid tearing the mirrors off.
- My Teflon™ chip-holder (see Figure 5.1) successfully protected the mirrors during their release and drying operations.

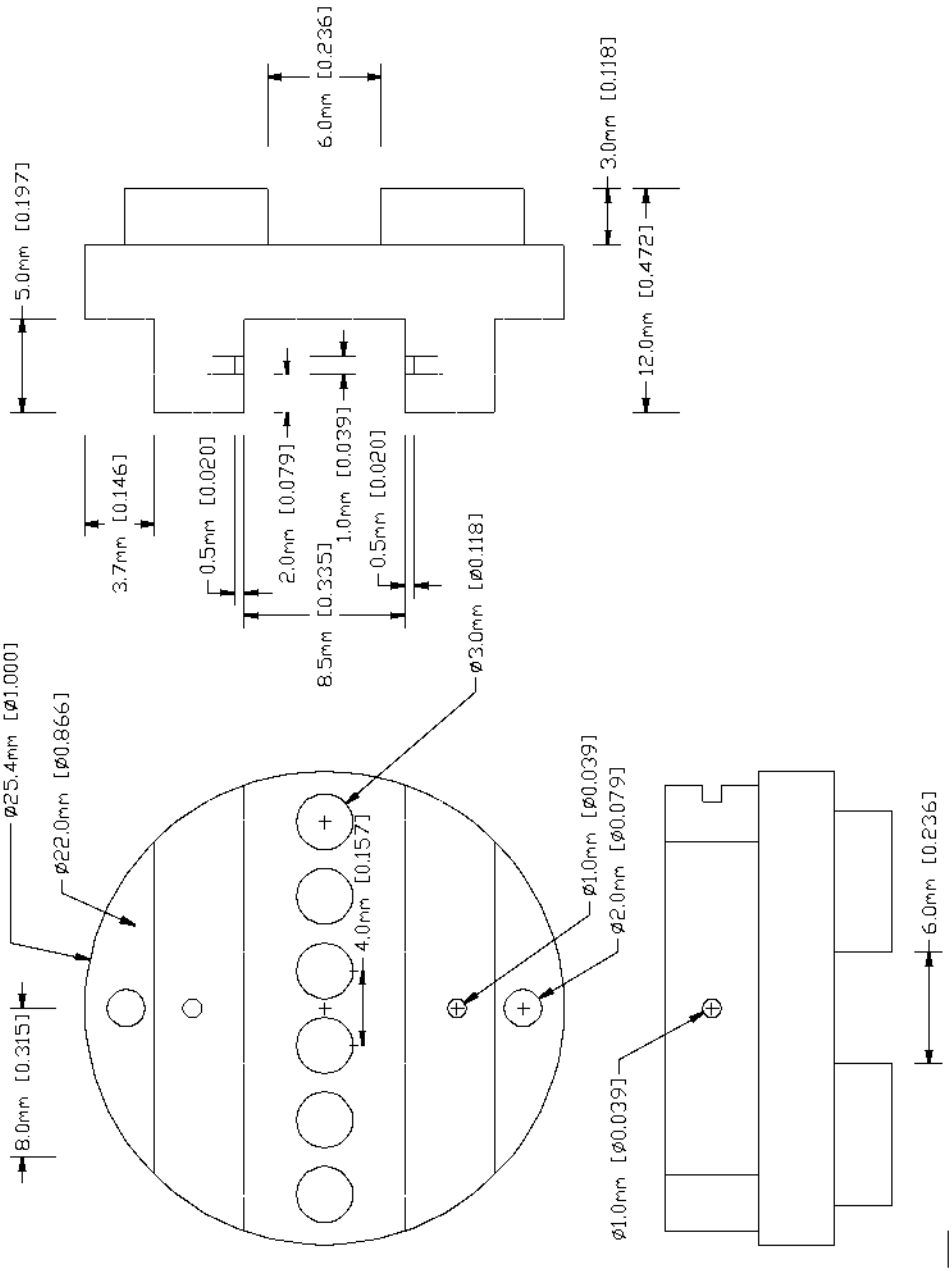


Figure 5.1 Release and drying chip holder.
This was made of Teflon™ to withstand HF acid.

5.2 DC Testing

Testing the finished fabricated chips began with applying an increasing DC potential between one of the address pads (left or right) and the mirrors on the device. Observing the mirrors while increasing the potential, we saw that the mirrors start to move and then, at slightly higher voltage, they snap down to the fully actuated position. The mirrors, when observed in a microscope, appear to darken because the illumination coming from the microscope objective is reflected outside the objective by the tilted mirrors. At extreme magnifications the effect is less obvious, since the numerical aperture of high-magnification objectives approaches one. Figure 5.2 shows three blue mirrors actuated. (I call the left mirror in each pixel, *red*, the center one, *green* and the right one, *blue*. The mirrors are not actually colored, but these names simply refer to the color of light that they are intended to reflect into the projection lens.) The mirrors actuate at different voltages. As the voltage is increased, more and more mirrors move, as is shown in Figure 5.3. The lowest actuation voltages are probably due to a few small defects in the springs, that have been observed on torn-up mirrors.

On some arrays, there are mirrors that never actuate as the voltage is increased. These mirrors fall into two groups: mirrors whose springs are simply too stiff to actuate, and mirrors whose underlying address pads are not making contact with the column conductors. Some entire dies were found to have no connections between the address pads and the column conductors, even though larger contacts between peripheral conductors could be verified. Apparently, the contact etch was not long enough to clear all of the LTO, or, more likely, the HF used to remove native oxide from the lower polysilicon layer failed to penetrate some of these contact holes. On an array where 97% of the mirrors actuated at 17V, the remaining mirrors did not actuate at 60V, implying that their springs are not just slightly stiffer.

Catastrophic failure occurs at around 70 V on the red and blue mirrors and at 30 V on the green mirrors. The failure mode seems to be an arc-weld, as most of the mirrors relax and one or two mirrors are stuck down, and the resistance between the driven lines drops from an open circuit to a few thousand ohms. Sometimes probing the stuck mirrors will release them, restoring operation. More often, this just breaks the mirror or the spring, rendering adjacent structures useless as well.

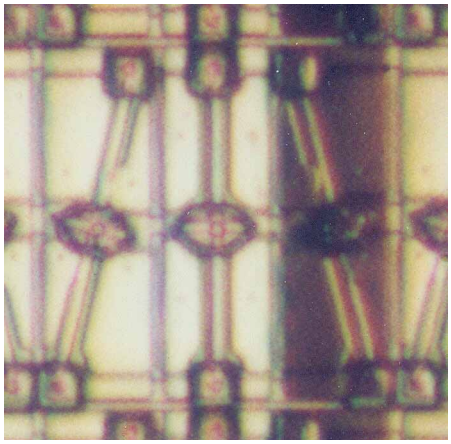


Figure 5.2 Blue mirrors actuated on sub-die 13 at 43 V

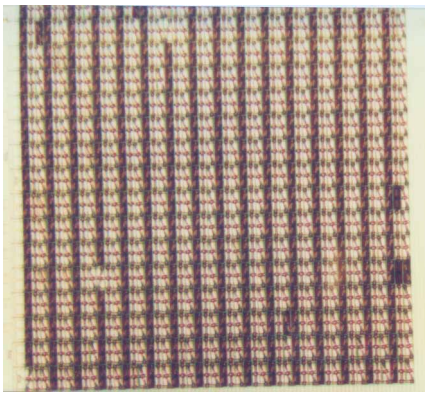


Figure 5.3 All but four of the red mirrors are active at 63.3 V on sub-die 13. Notice that three blue mirrors and two green mirrors are stuck from previous tests. One red mirror still had not actuated when failure occurred at 70 V.

The various sub-die each exhibit different actuation characteristics, as expected. The sub-die that feature stringer springs (3, 7, 11, 15, 19, 23) operate at much lower voltages than anticipated. Figure 5.4 shows what happened when an ohm-meter applied a small voltage to sub-die 15. Figure 5.5 shows the stringer springs that remained attached when a single mirror was ripped out of position.

The green mirrors failed to work because the address pads extend too far out, so that when the yoke failed to stop the mirror motion, the mirrors landed on the addressing pads, shorting the drive voltage supply and welding the mirrors down. This happened at

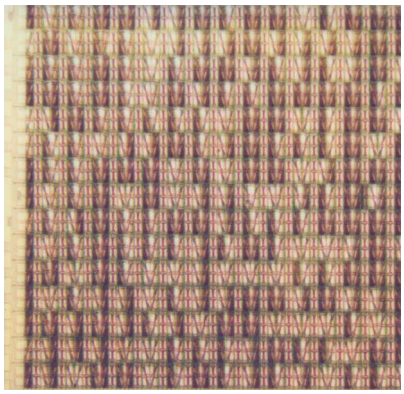


Figure 5.4 Stringer spring sub-die with an ohm-meter connected. Random pixels are actuated by the small voltage supplied by the meter.

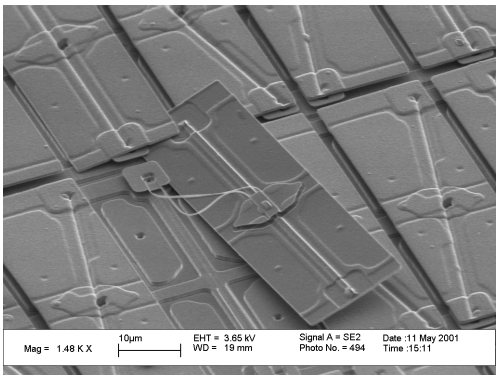


Figure 5.5 Stringer springs are visible still connected to the mirror on the upper side and disconnected from the yoke on the lower side.

such a low voltage that only about 5% of the mirrors had responded by the time a short occurred. On sub-die 13 the short occurred at 30 V.

The arrays without thick yokes seem to work best with 1500Å-thick springs. Figure 5.6 shows one of these arrays; all the red mirrors were actuated at only 17.7 V. Some of

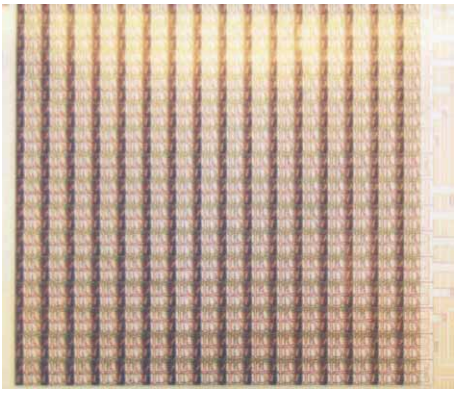


Figure 5.6 All red mirrors active on sub-die 22 at 17.7 V

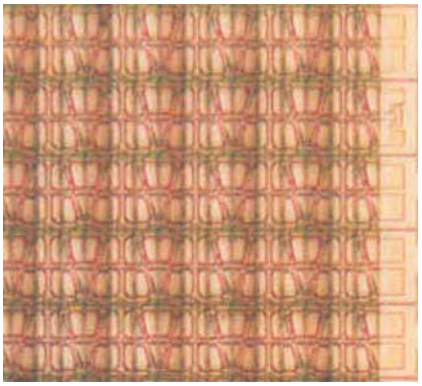


Figure 5.7 Square-wave drive at 20 Hz 10Vp-p, sub-die 22

these same mirrors are shown in Figure 5.7 being driven with a square- wave; the net effect is that about one-half of the light is lost on the red mirrors.

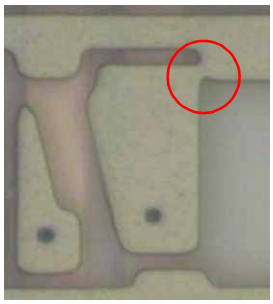


Figure 5.8 Short between address pad and row conductor at the edge of an array

Shorts at one edge of all the arrays between address pads and row conductors tie all the rows together and render the column useless. An unintended design-rule violation and underexposed photoresist combine to form these shorts, as seen in Figure 5.8. This made it impossible to test row-by-row addressing. In the planned operation, all the row conductors except the one row currently being addressed would be kept biased to hold the mirrors in their current position. This short also prevented tilting the blue mirrors to the right in even-numbered sub-dies, and red mirrors to the left in the odd-numbered sub-dies. The design rule violation occurred where the row conductors reached the edge of the array. In the center of the array the row conductors extend to the tiling boundary of the pixel, which is just one micron past the edge of the addressing pads. When the pixels are tiled together this leaves the required two microns between the pads. However, at the edge of the array, I connected the row conductors to much wider conductors (to reduce resistance) without remembering to leave an extra one-micron space between the conductor and the pad. I discovered later that longer photoresist exposures (nearly double what the Microlab staff was recommending) of the I-line resist would have cleared the resist in these one-micron gaps and prevented the shorts. The criterion that I had been using to establish exposure times was the minimum time that would clear the resist from open areas. In tight spaces, the less-than-perfect focus of the stepper means slightly less light hits the resist near the edges of features and thus the resist cannot clear during development. Once I started looking at the minimum features that were printing to establish the exposure time, I started getting much sharper resist patterns.

The actuation curves in Figure 5.9 summarize the DC actuation testing, showing that the device behaviors can be lumped roughly into four groups corresponding to the spring design. Each set of data points represents a particular mirror set on a sub-die. The

data points show how many mirrors were active out of a possible 256 at the voltage on the x-axis

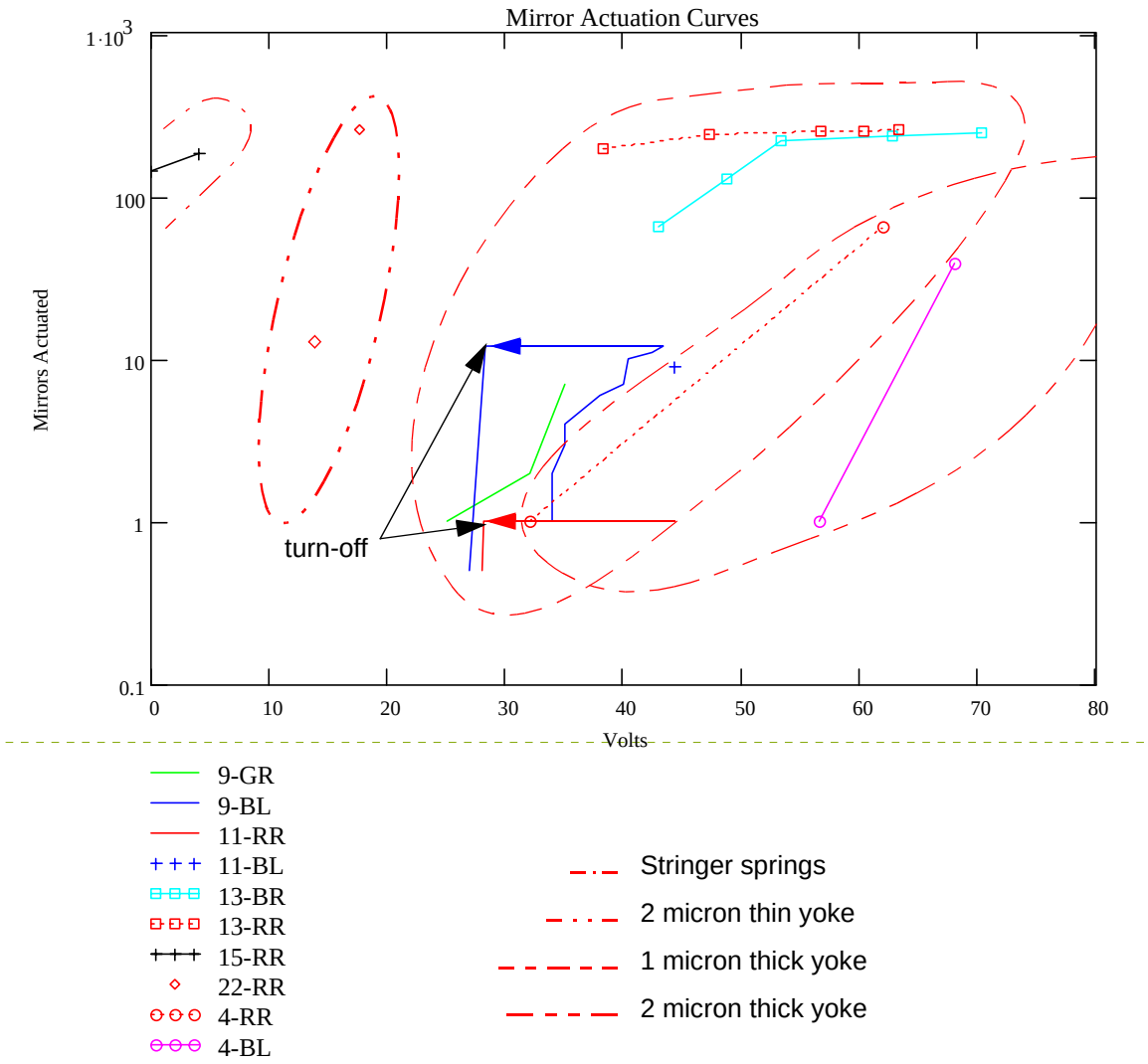


Figure 5.9 Mirror actuations vs. voltage.
Key gives sub-die number - color (R,G,B) and side driven (L,R).
Turn-off behavior shows on 9-BL, 11-RR, and 15-RR.

Assessing these tests, I would like to see springs just a little bit stronger than the two-micron-wide thin-yoke springs, as the mirrors in this group sometimes exhibit stiction. The springs in the thick-yoke groups are all far too stiff, but that is to be expected with these 1500Å-thick springs. If the springs had been fabricated at the designed thick-

ness of 900Å, the thick-yoke designs would have worked much better. At that thickness, the thin-yoke would be too flimsy to function. If the springs were thicker, then the stringer springs might function well.

5.3 Laser Doppler Interferometric Vibrometer Tests

The laser Doppler interferometric vibrometer (LDIV) allows measurement of z-axis (or out-of-plane) velocity on MEMS structures. This Polytec vibrometer (Model OFV-3001), has a new microscope adapter (Model OFV-074), that allows the laser spot to be focused onto the mirrors of the chips. The laser interferometer (Model OFV-501), supplies the laser beam through a fiber optic cable to the adapter that mounts onto the camera fitting of the microscope. A beam splitter in the adapter allows a video camera to view the chip while providing an optical path to the laser. Lenses in the microscope adapter focus the laser to a spot in the image plane that the microscope then projects onto the surface to the chip. The laser light reflected from the chip returns through the microscope's optics to the fiber and back to the interferometer. The spot size on the chip is a function of the microscope objective. Control knobs on the adapter allow the spot to be positioned within the field of view. Since my devices tilt so far, a fairly high-magnification lens is required so that the reflected light is not all lost. With a 25X objective on the Baush & Lomb Microzoom-II microscope, a spot size of about 3μm in diameter is obtained.

The instrument translates the frequency of the interference between the laser light bounced off the measured object and a reference beam, into a voltage proportional to the velocity of the measured object that is positive when the object is moving toward the laser. This velocity signal can be integrated by a digital oscilloscope to give a position waveform; however, small velocity signal offset voltages result in sloping position waveforms.

Tests in Room Air. These tests, in a normal lab atmosphere, explore the speed of operation and resonant behavior of the different spring designs. Large-voltage sine waves are

used to find operating threshold voltages, square-drive signals are applied to explore the large-signal behavior (normal operating mode), and small sinusoidal signals are applied to find resonances. Early tests were performed with the mirrors grounded and the drive signal applied to the address pad on one side of a mirror. The drive signal included a DC offset to keep the voltage positive and prevent the device from actuating twice per cycle.

Sub-die 2 was the first to be tested. A scanning-electron micrograph (SEM) of the underlying spring structures of this sub-die is shown in Figure 5.10. Figure 5.11 shows the

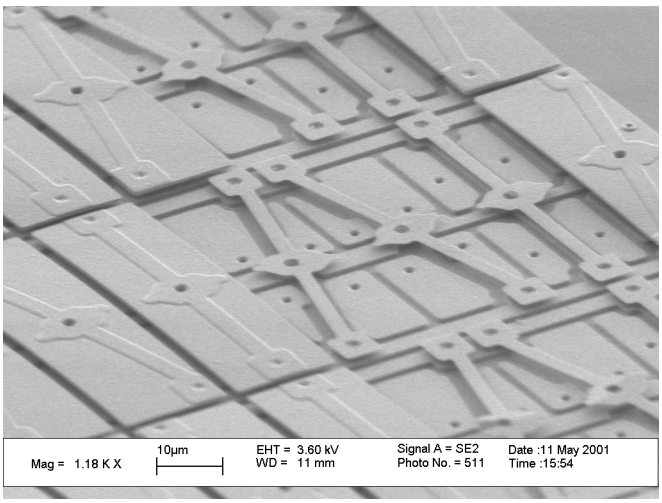


Figure 5.10 SEM of thin yoke springs
Note how flat the address pads and springs are.

velocity and drive waveforms for a 20 kHz drive signal applied to a blue mirror in sub-die 2. From the polarity of the velocity signal we can tell that the measurement spot is on the opposite side of the mirror from the driven address pad: the mirror is moving up toward the objective lens as the voltage reaches the threshold, and down when the drive voltage is being lowered. We can see that the mirror completes its motion (ignoring the ringing) in about 5 µs. An approximate integration of the velocity curve shows that the spot being measured moved over a range of almost one micron. The ringing has a period of about 4 µs, yielding an estimated resonant frequency of about 250 kHz. I attribute the ringing to a

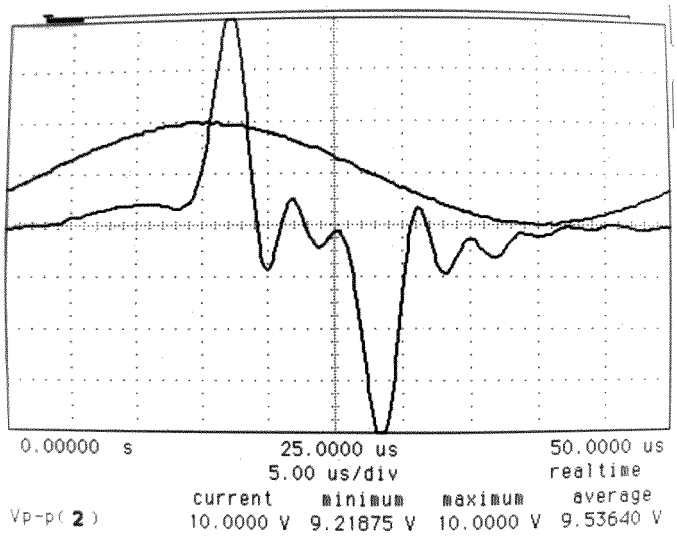


Figure 5.11 Mirror velocity and drive signal
Sub-die 2 Blue; 0-20V - 20kHz drive; 50mm/s/div; 0.2 µm/µs peak velocity

resonance of the torsion spring and mirror mass because the periods appear to be the same for both actuation and release.

Figure 5.12 shows the position of the mirror surface as a function of time, obtained by integration of the velocity in an HP digital oscilloscope, to give position. The resulting position trace slopes downward, indicating that there was a small negative offset error somewhere in the measurement system. The drive signal was not perfectly square because a 20kΩ resistor was put in series with the signal generator to protect against shorts. This waveform recorded the driven side of the mirror (because the mirror goes down when the drive voltage is applied). The position waveform is not symmetric; on the downward motion, there appears to be an exponential curve as the mirror approaches the address pad even though the electrostatic force is increasing. I attribute this deceleration to the "squeeze-film" effects of the air that must be pushed out of the way.

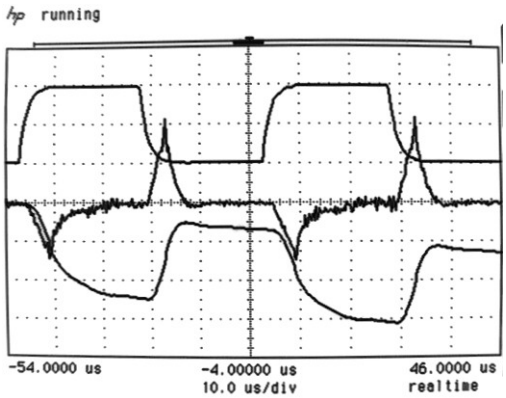


Figure 5.12 Oscilloscope calculated position vs. time.
Sub-die 2; red-right; drive=20kHz 4.5V to14.5V (top);
velocity: 500mm/s/div (middle); position: 1.0μm/div (bottom)

Gary Fedder, in his thesis[78], calculates the moment from squeeze film damping for a rectangular plate rotating about its y-axis (such as my green mirror) as:

$$M = \frac{-\mu L_y L_x^5}{60 z_0^3}\dot{\phi}, \qquad 30$$

where μ is the viscosity of the air, L_y and L_x are the dimensions of the plate, z_0 is the height of the rotational axis above of the surface and ϕ is the tilt angle. For my green mirror this would give:

$$M = \frac{-(1.79\times10^{-5}\text{Pa-s})(58\times10^{-6}\text{m})(18\times10^{-6}\text{m})^5}{60(2.8\times10^{-6}\text{m})^3}\dot{\phi} = -1.5\times10^{-18}\text{N-m-s}\,\dot{\phi}. \qquad 31$$

The peak velocity observed is about 1m/sec. Since the measurement point on the mirror was about half way out to R_{max}, we can estimate the rate of angular change as:

$$\dot{\phi} = \frac{v}{r} = \frac{1000\text{mm/s}}{10\mu\text{m}} = 100000\text{radians/sec}. \qquad 32$$

When we substitute this into Equation 31, we obtain -0.15pN-m. This is on the same order of magnitude as the electrostatic torques that drive the mirrors (found in Figure 3.11), approximately 0.5pN-m.

To simplify the Navier-Stokes equation, Fedder made the assumptions that the motions are small with respect to z_0 and that the velocities are low, neither of which is true in this situation, so actual damping forces are probably larger than the calculation shows. On the other end of the travel, as the mirror returns to its level position, we see only a very small overshoot and no measurable ringing, so the damping forces must be a factor. I cannot attribute all the behavior we see there to damping; some of it must be due to the touchdown of the yoke and mirror tip, and the subsequent storage of mechanical energy into the flexure of these structures. Such energy storage would account for the rapid acceleration and higher peak velocity of the mirror leaving the surface.

Moving to one of the mirrors with thick yokes and a one-micron spring, we need to raise the bias voltage to actuate it. An SEM of this type of yoke and spring is shown in

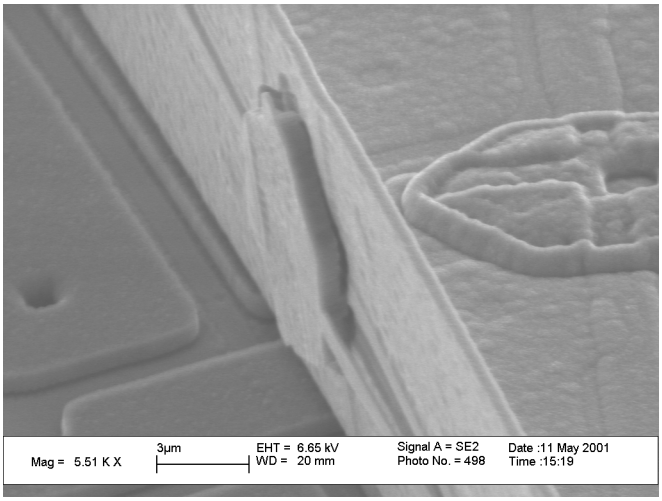


Figure 5.13 SEM of thick yoke with a 1µm spring on a ripped-up mirror

Figure 5.13. Between Figure 5.14 and Figure 5.15 we simply raised the bias voltage to get into a new mode. The point of measurement was on the non-actuated side, going up when the device was actuated. In the left half of each of these figures, the mirror returned to its level position and resonated at its natural frequency of approximately 200kHz. On the right half of each of these figures, the behavior is very different. Figure 5.14 shows ringing

on actuation at approximately the same frequency as upon release, while Figure 5.15 shows an entirely different behavior. First notice that the actuation time is considerably shorter and the velocity is higher due to the higher drive voltage. The most noticeable feature is the nearly doubled ring frequency. This higher frequency mode can be attributed to the mirror corner being pulled down against its landing pad. Once the corner has landed the mirror itself starts to resonate. If this interpretation is correct, then this higher voltage mode should probably be avoided to prevent the mirror tips from sticking.

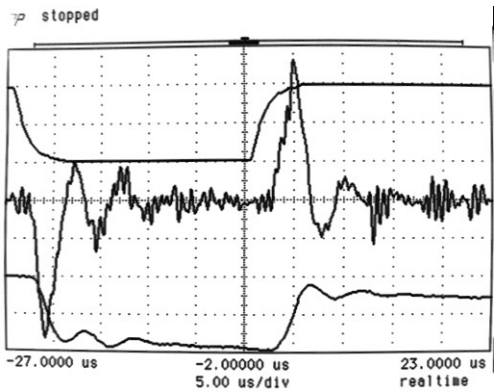


Figure 5.14 Mirror ringing slowly
Sub-die 9, blue-left;
Drive: 17.8V to 27.8V, 20kHz (top);
Velocity: 250mm/s/div (middle);
Position: 1.0µm/div (bottom)

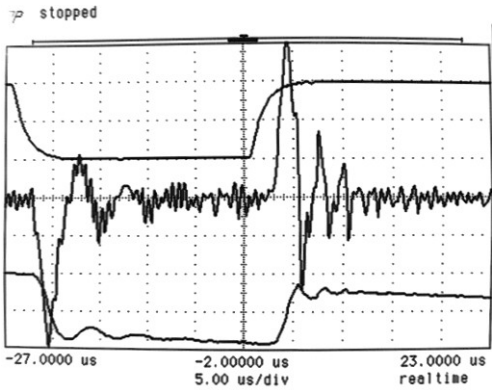


Figure 5.15 Mirror ringing fast
Sub-die 9, blue-left;
Drive: 20V to 30V, 20kHz (top);
Velocity: 250mm/s/div (middle);
Position: 1.0µm/div (bottom)

In Figure 5.16 and Figure 5.17 we compare the behavior of mirrors with thick yokes and two-micron torsion springs, with and without the landing springs. These two devices can not be claimed to be otherwise equal, as the drive voltages were quite different. The ringing after the mirror lands is much less in Figure 5.16 with the landing springs.

This would seem to show that the landing springs do at least absorb energy on landing. (Their main purpose is to lower stiction.)

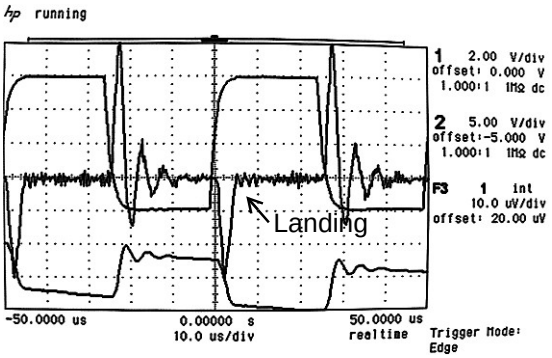


Figure 5.16 With landing spring
Sub-die 12, red-right;
Drive: 38V to 58V, 20kHz (top);
Velocity: 50mm/s/div (middle);
Position: 0.25μm/div (bottom)

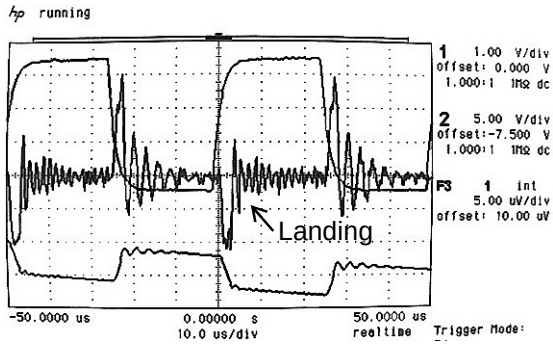


Figure 5.17 Without landing spring
Sub-die 24, blue-left;
Drive: 28V to 48V, 20kHz (top);
Velocity: 25mm/s/div (middle);
Position: 0.125μm/div (bottom)

Two of the vertical (or stringer) spring mirrors were operated at very low voltages (see Figure 5.18 and Figure 5.19). Since these were both green mirrors, they shorted out their arrays as the drive voltages were increased beyond those shown. We can see that the air damping is keeping the mirrors from resonating, The position trace on Figure 5.19 shows a corner that resulted from the yoke landing.

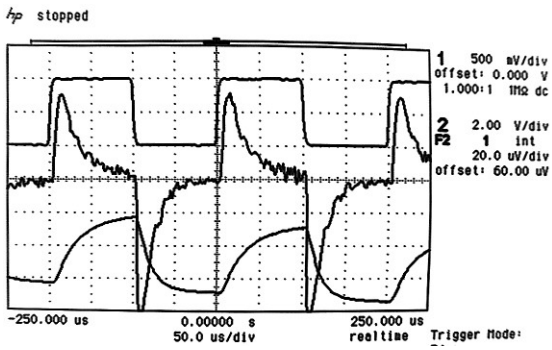


Figure 5.18 Vertical and landing springs.
Sub-die 11, green-left;
Drive: 2V to 6V, 5kHz (top);
Velocity: 2.5mm/s/div (middle);
Position: 0.1μm/div (bottom)

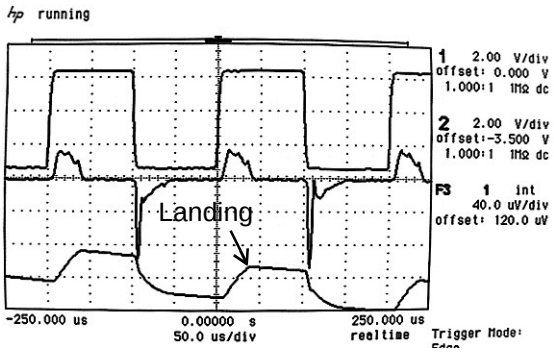


Figure 5.19 Vertical springs.
Sub-die 23, green-left (top);
Drive: 2.4V to 8.3V (middle);
Velocity: 10mm/s/div (middle);
Position: 0.2μm/div (bottom)

Two methods for scanning the frequency spectra of the mirrors were tried on sub-die 24 because it exhibited the strongest resonance in air. For Figure 5.20 I used a signal generator to sweep logarithmically through frequencies from 1 kHz to 500 kHz in 5 seconds. The oscilloscope sampled the drive and velocity signals (which is why they appear irregular). The velocity reaches a maximum near the end of the sweep, even as the drive signal is falling off due to the resistor in series with the signal generator.

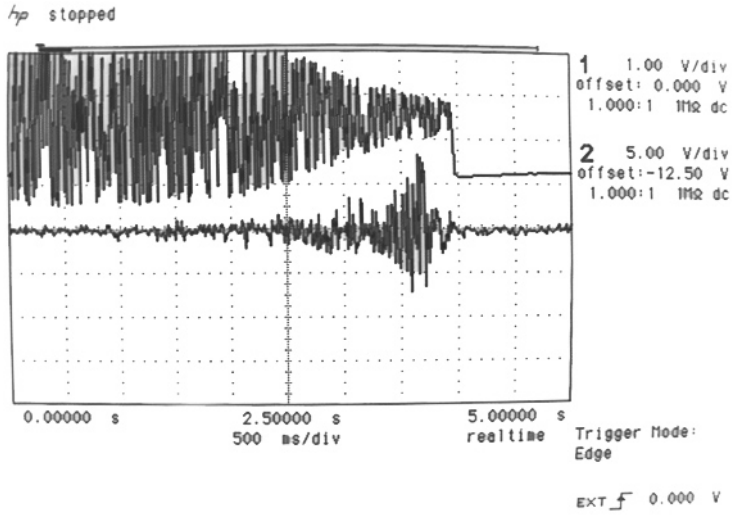


Figure 5.20 Frequency sweep 1-500 kHz.
Approximately 50 kHz/div; Drive signal 0.5V-20.5 V (top)
Velocity: 25mm/s/div (bottom)

Since this mirror seemed to be able to respond to a small signal, I connected a spectrum analyzer that can only provide a 1 V drive signal, and returned the output of the vibrometer to the spectrum analyzer. Figure 5.21 shows the resulting spectrum. The response recorded is the velocity, which is proportional to the amplitude times the frequency. The analyzer shows a peak response at 252 kHz.

One of the more subtle measurements that my advisor suggested was to find how much motion the air couples from an actuated mirror into an adjacent, non-actuated mirror. The signal from the vibrometer was buried in the noise, but after some filtering we found that the velocity on the adjacent mirror was 10 mm/s vs. 125 mm/s on the driven mirror.

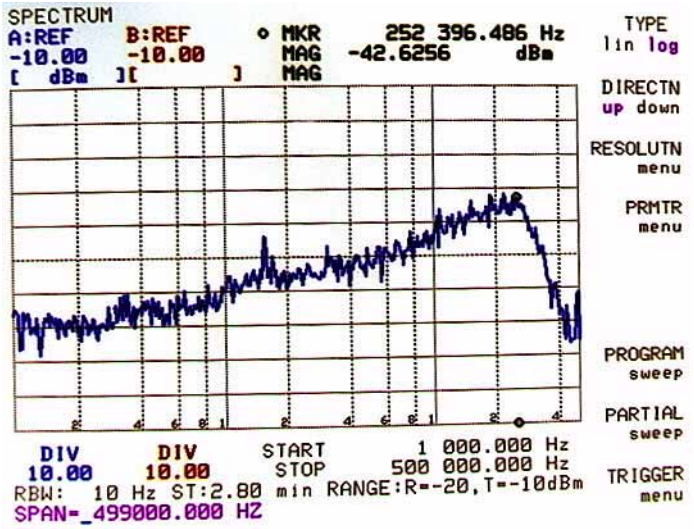


Figure 5.21 Spectrum analyzer display of mirror response

Vacuum Tests. The next series of tests was completed with the device running in the MMR Technologies, Inc. vacuum probestation. The vibrometer microscope adaptor was moved to the probestation, and a 25X objective was installed on the microscope. Because of the shorter working distance of this objective, I had to raise the die closer to the vacuum-chamber window using aluminum shims, and shorten the probe tips. The chamber reached a base pressure of 67 mTorr, about 0.0001 atm.

Four sub-die were tested, 11-14, representing one of each spring type. Frequency sweeps were made to find resonances and quality factors. Figure 5.22 shows a frequency sweep of sub-die 11, a vertical-spring mirror. Figure 5.23 shows it operating at resonance at 93.6 kHz. The measured Q is 90. Note that the estimates (from ringing) of the Qs of mirrors operated in air ranged from 1 to 9.

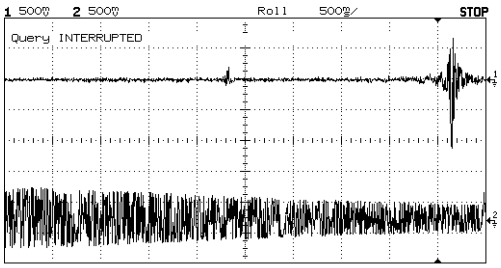


Figure 5.22 Frequency sweep — 11.
Velocity: 12.5 mm/s/div (top);
Drive: 0-100 kHz linear (bottom).

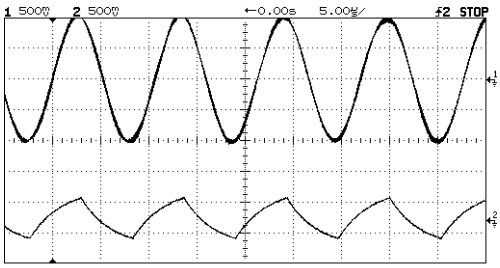


Figure 5.23 Resonance — 11.
Velocity: 12.5 mm/s/div (top);
Drive: 93.6 kHz, 0V to 1 V (bottom).

Table 5.1 summarizes the tests in vacuum. The thin-yoke mirror had a second resonant frequency at nearly 250 kHz, as seen in Figure 5.24 and as we observed earlier in the atmospheric testing.

Table 5.1 Resonant behavior in vacuum

Sub-die	Spring	Mirror	Drive (V)	F_{res} (kHz)	Q
11	vertical	green-right	0 to 1	93.1	90
12	2μm/thick-yoke	red-right	0 to 20	238	18
13	1μm/thick-yoke	blue-left	13 to 19	209	20
14	2μm/thin-yoke	red-left	-1.1 to 4.6	92	10

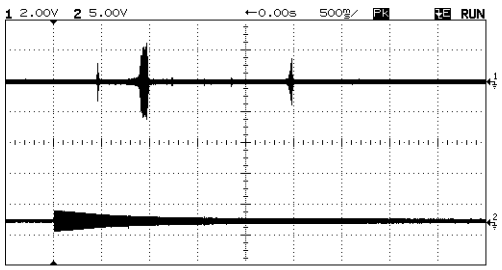


Figure 5.24 Resonances of sub-die 14.
Drive: 0-500 kHz; 50 kHz/horizontal-div; starts one division from the left edge.

The observed resonances correspond fairly well with expected resonance and are high enough to implement large screen displays.

5.4 Life Testing

An extended test was run on another die that was wire-bonded into a 24-pin dip ceramic package. The test ran 1030 hours, or almost 43 days. The red-right address pads on sub-die 18 (one of the thin-yoke devices) were driven with a 20 V peak-to-peak 500 Hz square-wave and the mirrors were biased to -10 V. The individual mirrors were cycled over 1.8 billion cycles to one side only. This test was designed to see if the springs would take a set like TI's. Exactly 146 mirrors were operational at the start of the test. Only 6 mirrors stopped actuating, and 15 became stuck in the actuated position during the test. Figure 5.25 shows an SEM of the device immediately after the test stopped.

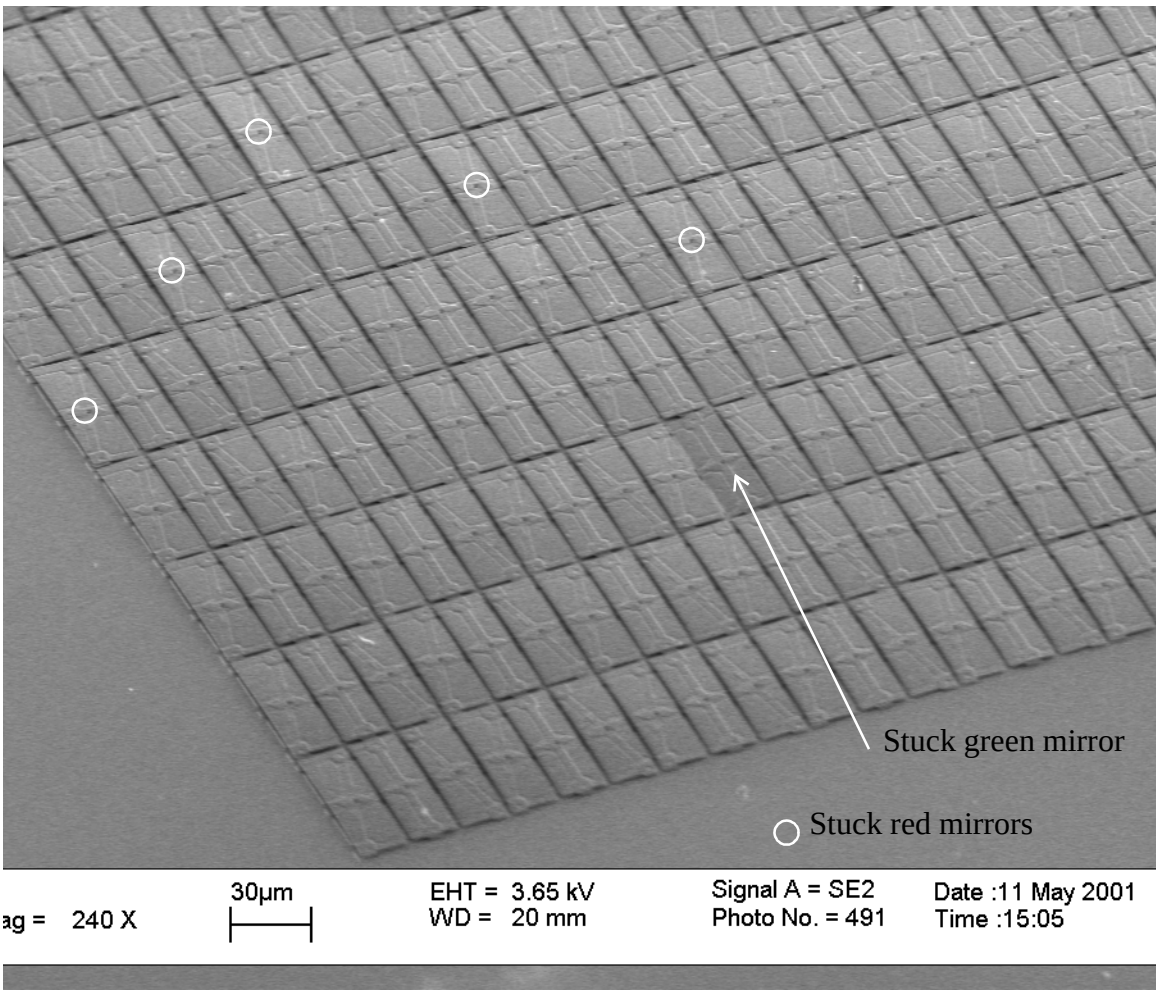


Figure 5.25 SEM of the life-test sub-die

No mirrors are visibly out of their level positions except those known to be stuck.

5.5 SUMMiT Tests

Here is a picture gallery of the nine designs The three hinged designs all appear to

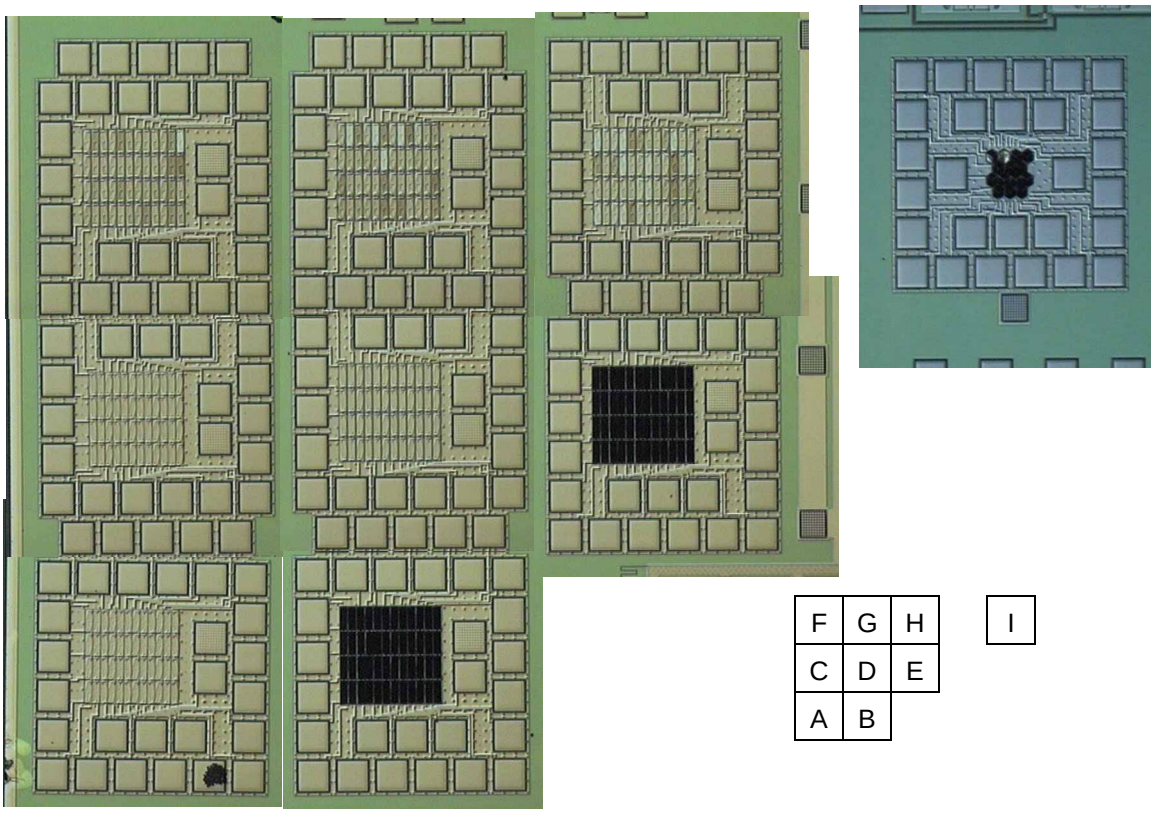


Figure 5.26 A collage of micrographs of the 9 designs from the Sandia run. Notice that the designs share bonding pads with their neighbors.

be black because the mirrors are tilted, and, at this magnification, return no light to the microscope. SEMs of the hinged designs are shown in Figure 5.28, Figure 5.29, and Figure 5.30.

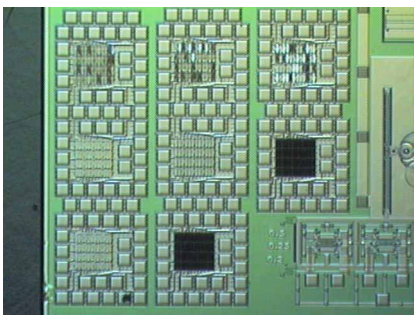


Figure 5.27 Low-magnification micrograph of “A”-”H”

The mirrors of Designs “F” to “H” (with spiral springs) are tilted slightly, and can be seen more dramatically at the lower magnification of Figure 5.27. The fact that the mirrors are not level to start with is a bad indication for the spiral springs.

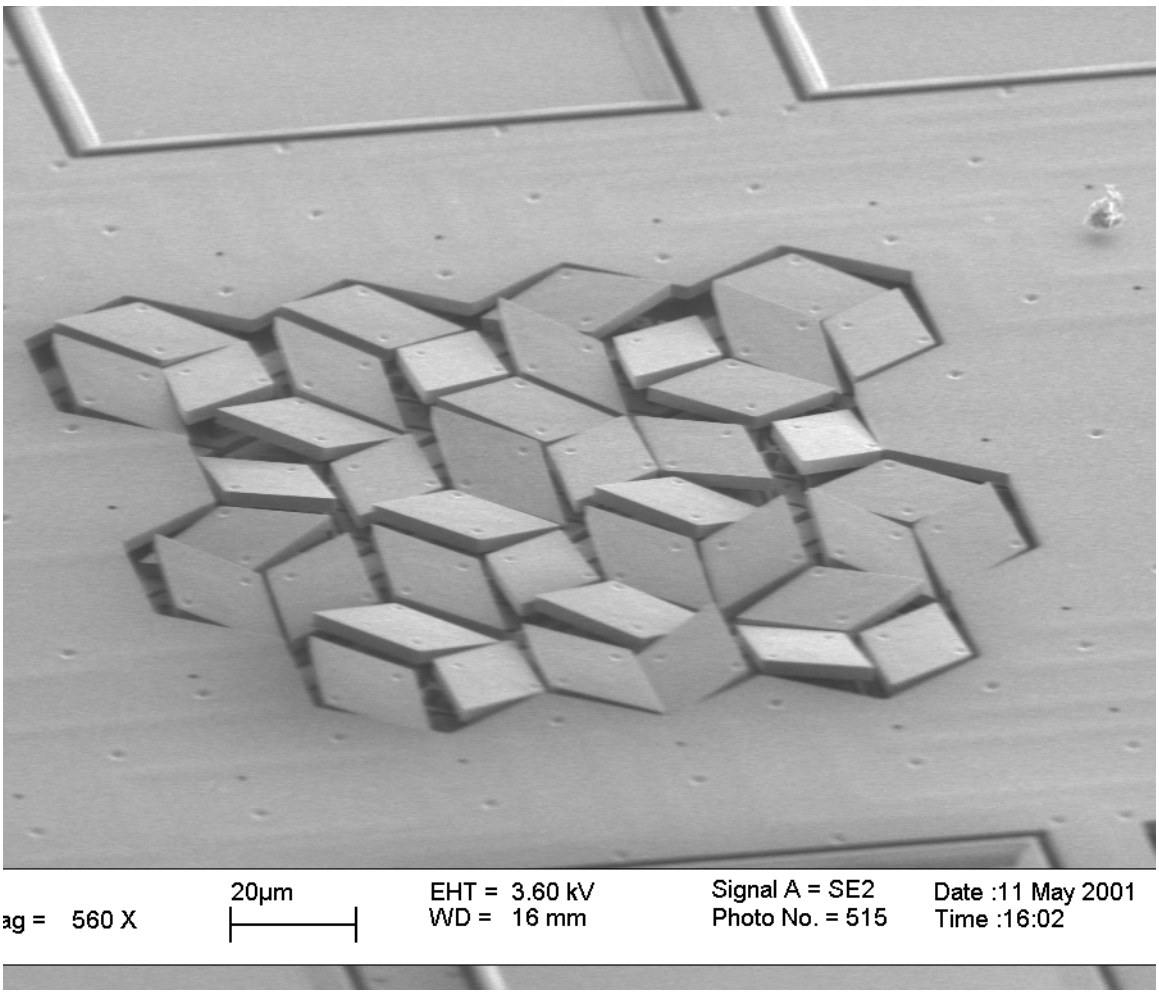


Figure 5.28 SEM of Design “I” with hinged hexagonal pixels.
The mirrors are in random positions from turbulence during release.

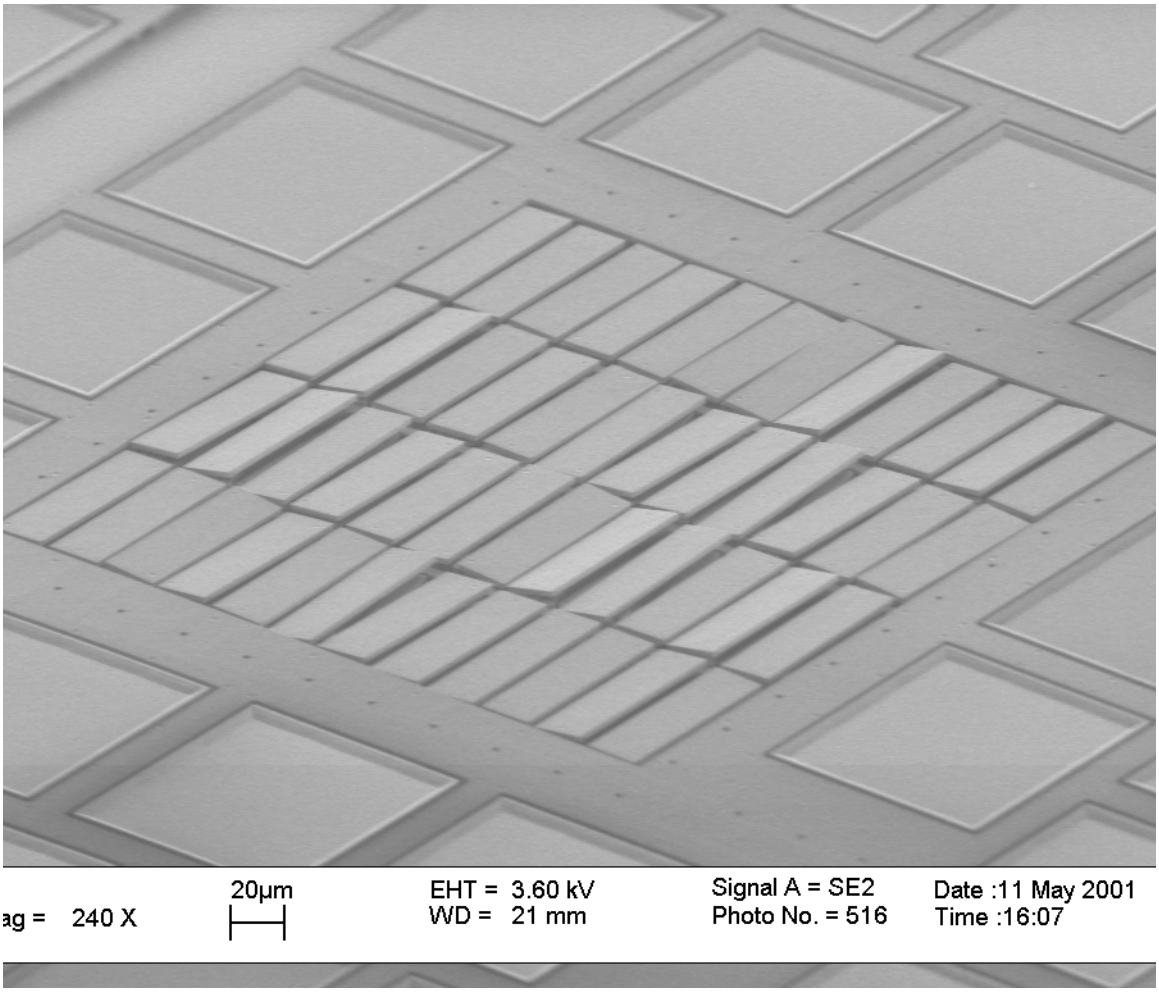


Figure 5.29 SEM of Design “B” with loose hinges

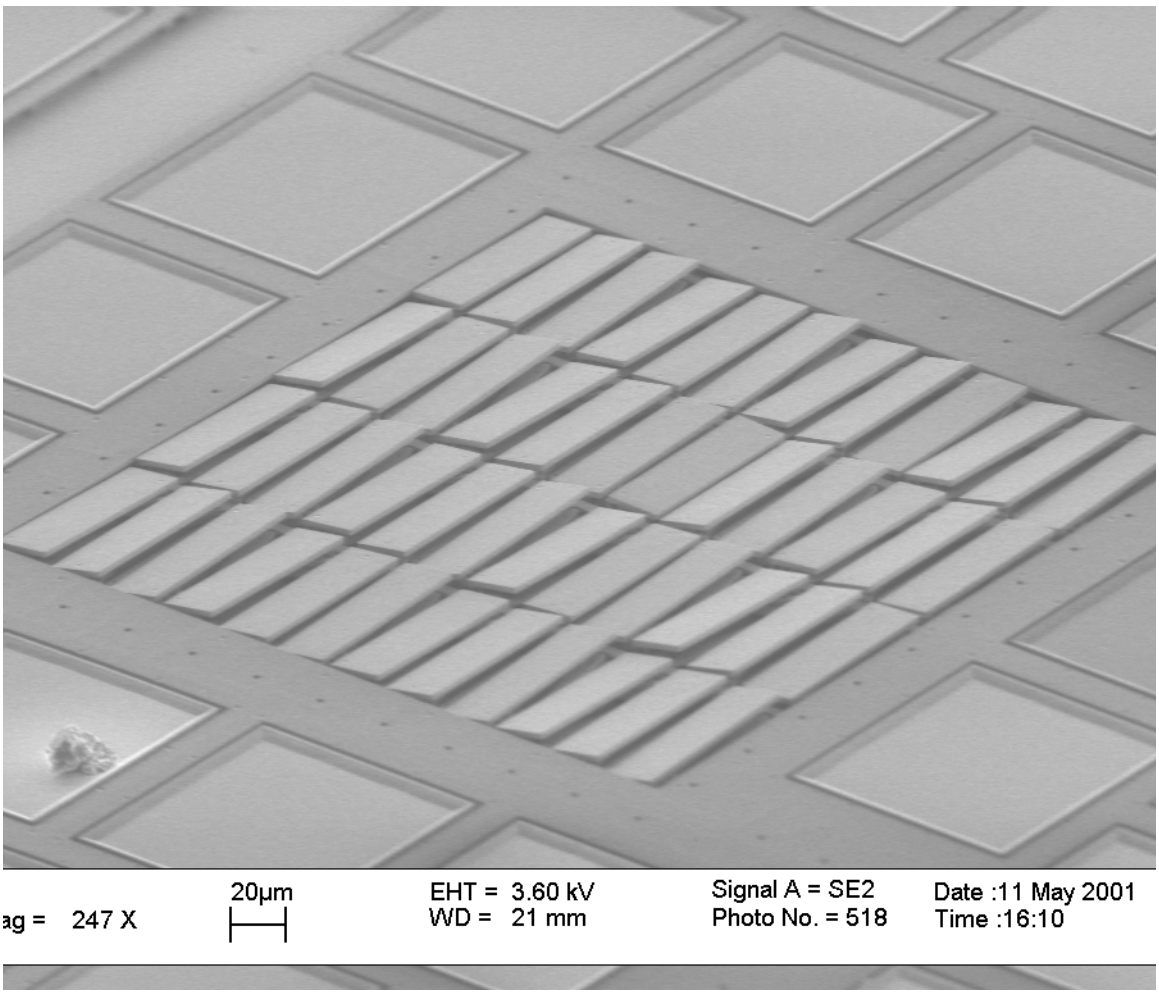


Figure 5.30 SEM of Design “E” with tight-tolerance hinges.
Note the dust particle on one of the bonding pads. Compare the size of the dust particle to the size of the mirrors, and imagine what would happen if the dust particle got under one of the mirrors. It is very important to protect these devices from dust and humidity.

Early DC-drive tests were limited to 40 V and only Design “F” responded. I was able to tilt one mirror on that array in both directions with 23 V. Later DC tests with up to 100 V moved mirrors on most devices, but welded them down.

The mirrors in Design “I” were observed to touch and even overlap each other, as I had forgotten to account for both lateral (along the hinge) and angular play (about the z-axis) in the hinge.

Using a probe on a micromanipulator I was able to move a mirror in each of the hinged designs, proving that the hinges were free. This is such a delicate operation that even with the micromanipulators I ended up breaking hinges by poking the mirrors. A micrograph of Design “I” in Figure 5.31 shows tilted mirrors.

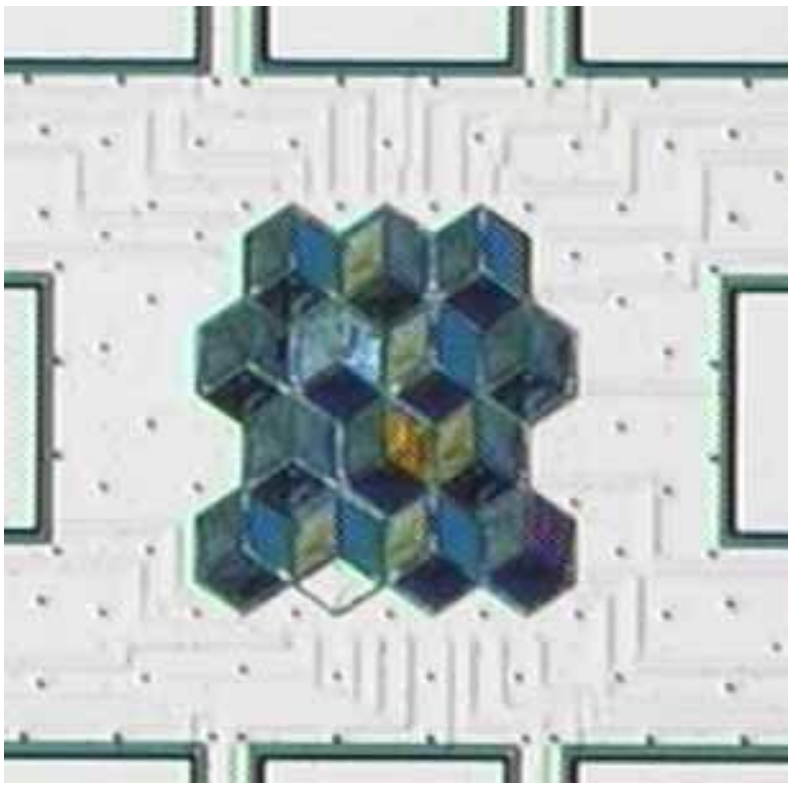


Figure 5.31 Tilted mirrors in hexagonal pixels — Design “I”

Using the LDIV, resonant behavior of these designs was measured. Figure 5.32 shows a frequency response for the red mirror on Design “A” (with the serpentine spring). As we would expect, the green mirrors have a different response, as shown in Figure 5.33.

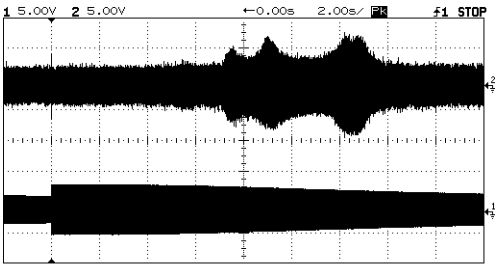


Figure 5.32 Frequency sweep of a red mirror on Design “A”

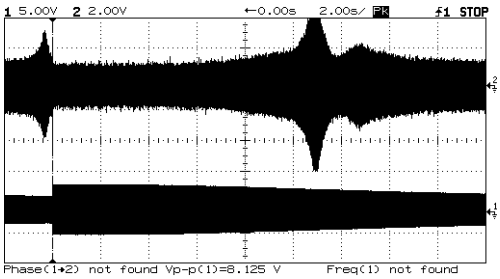


Figure 5.33 Frequency sweep of a green mirror on Design “A”

Similar sweeps were run on each of the designs; the summarized results are in Table 5.2. The difference between Designs “C” and “D” is that the mirrors are smaller on

Table 5.2 Summary of resonances of Sandia spring designs

Design	Red or Blue F_{res} (kHz)	Red or Blue Q	Green F_{res} (kHz)	Green Q
A	98.5	10	84.7	13
C	149	15	136	17
D	142	30	122	40
F	41	6	52	8
G	45.6	7	46	9
H	no resonance observed 0-400 kHz			

“D.” That would lead us to expect a higher resonant frequency, not lower, so these results are not what would be expected.

The spiral springs of “F” and “G” have substantially lower resonant frequencies, which is in line with our expectations because the springs were supposed to be softer.

It would appear that if we could resonate these mirrors using special drive electronics, we could “trap” them in a fully tilted position and thus be able to operate these devices without having to use excessively large DC-drive voltages. It would seem to be

necessary to fine tune the mask layout of the springs on the green mirrors to achieve matching resonant frequencies with the red and blue mirrors.

Finally, the hinged Designs “B” and “E” were driven with gradually increasing DC voltage to see if motion could be induced. The “B” array did not respond even with 120 V drive. The “E” array (with the tight-tolerance hinges) switched with voltages that initially started around 50 V and gradually came down to between 20 V and 30 V. The switching behavior was captured using the LDIV and an oscilloscope. Figure 5.34 shows two instances of one of the mirrors moving. The switching time of 20 µs would only work for a small display. This device, however, would be wonderful for a low-power black-and-white application (like a helmet display) as it could hold an image with no power.

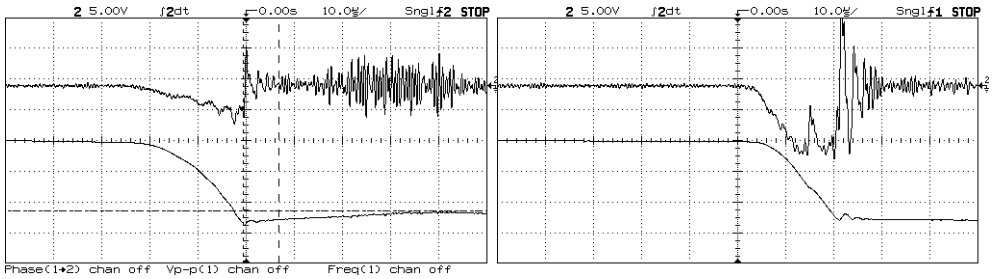


Figure 5.34 Mirror transitions on Design “E”
Velocity: 125 mm/s/div (top traces)
Position: scale approx. 1 µm/div (bottom traces)

6. Future Directions

In this chapter, I present some ideas for: refining the design to simplify the process, improving the process to increase the yield, and tasks for turning this design into a large-scale high-resolution projector. These tasks include scaling, flip-chip interconnection and drive circuit and refresh algorithm design.

6.1 Design Improvements

Hindsight based on the devices fabricated suggests that better design of the masks could eliminate the need for CMP after the LTO has been deposited over the addressing pads by running a row conductor underneath each torsion spring rather than just the center one. Since the nitride layer under the row conductors is already flat, the row conductors would be flat and the springs formed directly over the row conductors would thus be flat. This was precluded in the existing design by the margin around contacts on the smaller addressing pads.

The address pads under the green mirrors need to be made smaller to prevent their outside edges from coming into contact with the mirrors.

Modifications to the mask set should also be made to improve CMP performance. Specifically, modifications were made to the first poly mask to make the feature density uniform over the entire die. This idea needs to be carried upward through the design to balance the material removal load during CMP steps.

The bonding pads should only be on the second poly layer, in order to avoid issues with stringers and deep holes.

6.2 Process Improvements

The major process improvement that I would make is a native oxide removal step in the polysilicon deposition tube. This could be accomplished by bubbling nitrogen

through an HF solution and into the tube. This would cause some very minor erosion of the quartzware where it is not covered with polysilicon, but we only need to remove a few angstroms of material in each run. There is strong evidence that we are depositing poly on top of native oxide even after performing an HF dip in the pre-furnace wafer clean. Figure 6.1 shows a stringer of polysilicon that has pulled away from one of the polysilicon yokes. This could only happen if there were a layer of some other material on the yoke that was subsequently removed in the release etch. A vapor etch would also help improve the minimum-feature-size contacts that were rather inconsistent in my devices. Many of the mirrors that failed to operate simply were not connected.

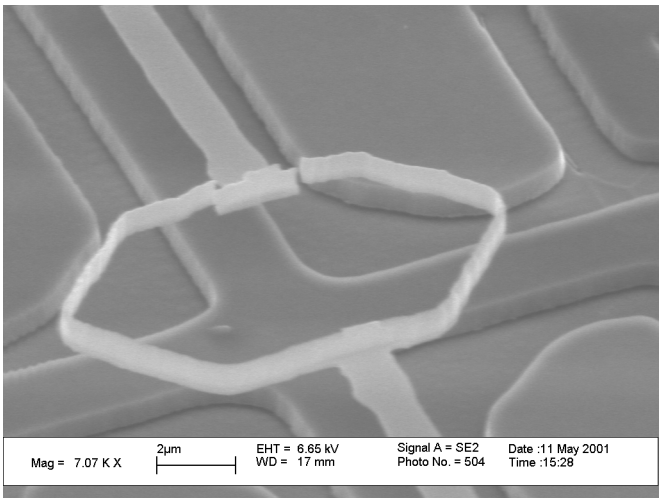


Figure 6.1 SEM of a polysilicon stringer separated from a yoke

CMP needs further development. Current cross-wafer uniformity is poor and yield is subsequently low. Perhaps the belt-style units now available commercially would work better.

6.3 Metallizing

The current process flow calls for aluminum or gold metallization on the mirrors. Experimental HF releases showed bad discoloration of the aluminum. Subsequently, I

have heard that the discoloration may be caused by photochemical reactions, and that etching in the dark will avoid the problem. I have not verified this experimentally. Using gold instead of aluminum may solve this problem, but there will be some loss of reflectivity. The best solution may be to evaporate aluminum onto the die after it has been released. (See “Metallization” on page 52.)

6.4 Scaling the Design

To make practical size devices that will not exceed the capabilities of lithographic steppers, and that will have reasonable yields, it will be necessary to scale down the current design. Figure 6.2 shows the resulting array size for standard display sizes. Clearly these would be too large to fabricate reliably. The current pixel size is as small as it could be made with the design-rules currently in use at Berkeley, but smaller pixels are needed. Shrinking the design raises three issues: minimum design rules, optical behavior, and scalablity.

The design rules for the current 60-micron-square pixel are 2.0 microns. A scale factor of 0.25 would bring the pixel size down to 15 microns, and require 0.5-micron design rules. This would result in the high-definition television (HDTV) array being nearly 3cm wide, which would be acceptable. The individual mirrors would only be about 5 microns wide. Scaling instead with a factor of 1/6, for a 10-micron pixel would perhaps be more attractive as the HDTV array would be just under 2cm wide. However, as the size decreases, diffraction effects increase, reducing the image contrast. Also as we scale down the x and y dimensions we will not be able to scale the mirror thickness, as there will be a minimum for good reflectivity.

Scaling the design will change the forces that are at work in the pixel. Actuation voltage is a based on the required force to overcome the spring torque, and that in turn is

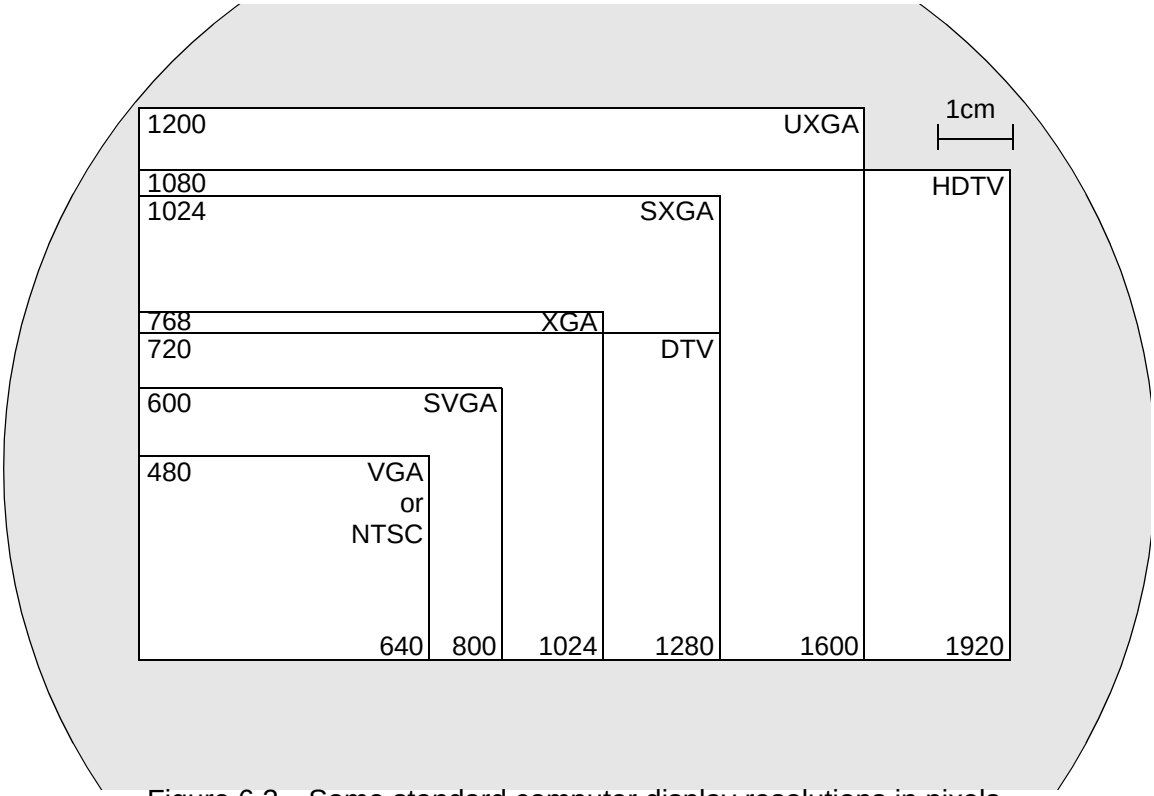


Figure 6.2 Some standard computer display resolutions in pixels and the size, shown to scale, if they were fabricated with 60μm pixels (against the background of a 6-inch wafer). Also shown are television resolution standards for NTSC, digital television (DTV), and high-definition television (HDTV).

determined by the force required to overcome stiction. The effects of scaling on stiction, capacitance, electrostatic force, and the spring constant are:

- The number of contact points and the contact angles are independent of scaling, so stiction should remain constant, but the torque required to overcome it would go down, because of the shorter working distance.
- The capacitances of the addressing pads will scale linearly downward: while the area will decrease by a square factor, the distance between plates decreases linearly, and so the net capacitance is proportional to the scaling factor.
- If the operating voltages are held constant, the charge on an address pad will decrease linearly with the capacitance, the field strengths will increase over the shorter distances, and their product, the electrostatic force, will remain constant.

The torque generated would drop because of the shorter distance over which the force is acting.

- We can adjust both the width and thickness of the springs to meet the torque requirements. As we shorten the spring, the spring constant increases linearly, but narrower springs have a lower spring constant; the two effects nearly cancel. The thickness of the spring cubed is a major component of the spring constant, so we will need to reduce the thickness only slightly to achieve the lowered torque requirement to overcome the stiction.

It looks like we would not be able to lower the operating voltages as the device scales down, unless something else is done to reduce the stiction, or we use dynamic "reset" pulse tricks that Texas Instruments employs to overcome the stiction[55][63][70][71].

So what happens to the operating speeds as we scale down? The answer lies in the resonant frequency of the spring and mirror. It is impractical to reduce the mirror thickness, but the mass of the mirror will be proportional to the square of the scaling factor. Resonant frequency should, as a result, increase as the inverse 3/2 power of the scaling factor. This means we will have faster switching that will enable larger displays to be realized.

6.5 Interconnections

Since this design doesn't require active circuitry on the MEMS die, drive circuits will have to be flip-chip bonded onto the periphery. The number of connections that will be required is prodigious. Each pixel column requires six connections, and each row requires one. A large display whose number of lines is not an integral power of two will most likely be driven from the top and the bottom as if it were two separate displays. Driv-

ing both will nearly double the number of required contacts. As and example, an HDTV-resolution display with 1920 columns and 1080 rows, would have a contact count of:

$$1920 \times 6 \times 2 + 1080 = 24120 \ ! \qquad 33$$

Clearly, this is not a device that you could put into a package without the drivers, as the number of pins would be a couple of orders of magnitude larger than is practical. Once the drive circuits have been provided, data can be supplied serially at high frequencies and a very low total pin count can be realized.

6.6 Drive Circuits

The aggregate bit rate that is need to supply the columns can be found from:

$$\text{bit\_rate} = \text{columns} \times 3 \times \text{rows} \times \text{color\_depth} \times \text{refresh\_rate}, \qquad 34$$

where color_depth is the number of bits used to represent each color, and rows is the power of two that is less than or equal to the actual number of rows in the display. For an extreme HDTV display, the bit rate becomes:

$$\text{bit\_rate} = 1920 \times 3 \times 1024 \times 10 \times 30\,\text{Hz} = 1{,}769{,}472{,}000\ \text{b/s}. \qquad 35$$

That may seem to be a very large rate, but by feeding 32 data bits in parallel to the chip, the clock rate could be reduced to a reasonable 55.296 MHz.

Each column would require three drive circuits, one for each mirror, to drive the column conductors to 5 V logic levels. Each drive circuit would need a latch to hold the value currently driving the column and to provide the complementary logic levels to two buffers — one for address electrodes on each side of the mirror. In addition, each drive circuit would contain a single bit of the shift register used to receive the incoming data for the next line while the current line is being addressed. A schematic drawing of a single drive circuit is shown in Figure 6.3.

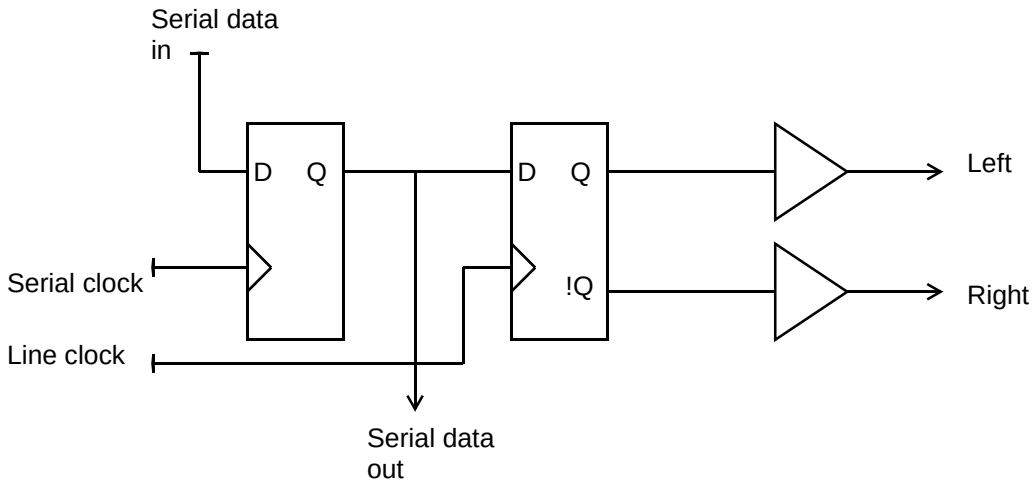


Figure 6.3 Schematic of a column driver.

6.7 Refresh Algorithm

In Chapter 1 we discussed the concept of pulse-width modulation (PWM) to achieve the required brightness levels from each pixel. We would expect to combine PWM with the overall frame refresh while maintaining a uniform rate of data flowing into the chip, Figure 6.4 is key to understanding how to accomplish this combination. The figure shows time progressing from left to right, and the rows of the display vertically. The entire time period shown is just one frame refresh period. The frame period has been broken into equal pieces (line periods), one for each row of the display. Each line period is further broken into equal pieces, one for each bit in the grey-scale binary code that we are using for each mirror. These bit times are not indicated by lines in the figure, but rather by the positions of the individual digits that appear in the line-period slices. Each line period delivers each of the bit values to some line in the display; the magic is in which one. The value of each bit position, n, in the grey-scale code needs to remain on its row for 2^n line periods before being replaced.

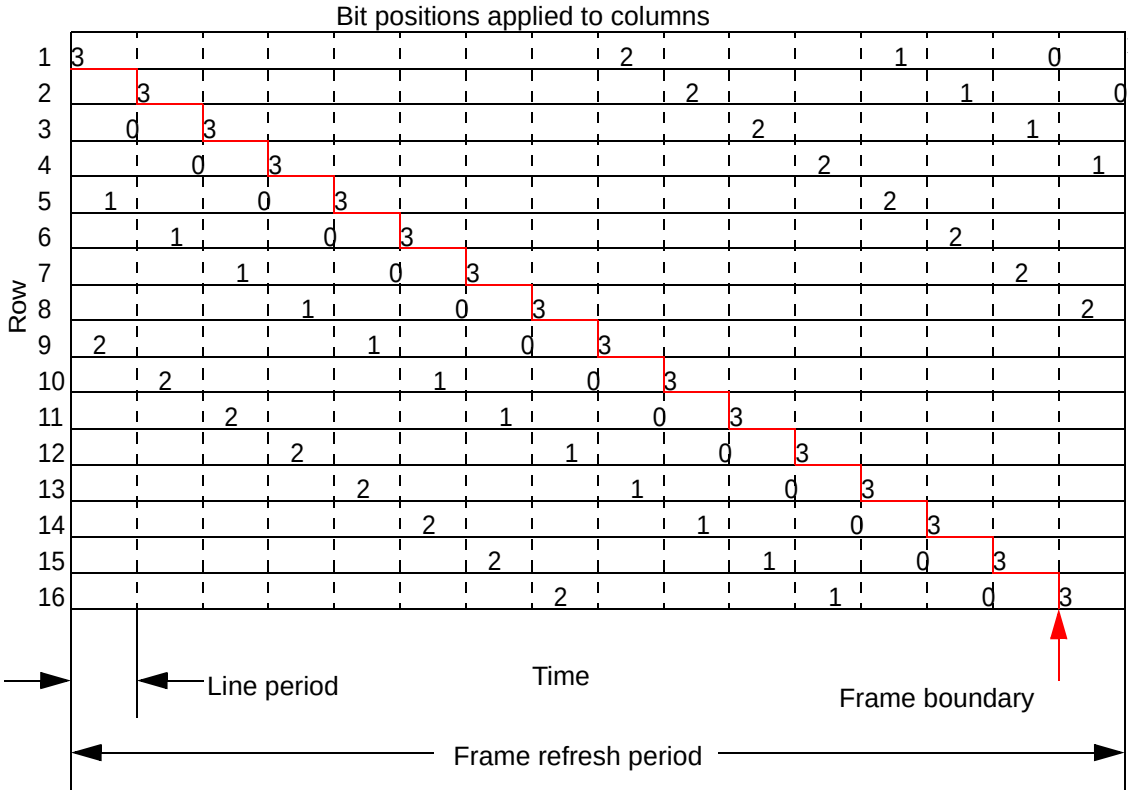


Figure 6.4 Frame refresh algorithm that incorporates pulse-width modulation. Illustrated for a 16-line display with 16 levels of brightness.

One can count line periods from left to right in any row to see that the times are as required. It may look as though the zero bit is on for too long, but it starts in the last bit-slice of one line period, continues for the entire next line period, and is replaced by the most significant bit in the first bit-slice of the next period. This is a total of $(1+1/m)$ line periods, where m is the number of bits in the grey-scale code. In fact, careful examination shows that each bit is on for a period of $(2^n+1/m)$ line periods. We can reconcile this with the fact that the mirrors take a approximately $1/m$ line periods to move from one position to the next.

If a display size is not a power-of-2 number of rows, the solution is to divide the rows into two groups; the top group of rows will have the largest power-of-2 that will fit, and the bottom group will have the rest of the rows. The bottom group will be treated as if

it were its own display with exactly the same number of lines as the top group. The bottom group will receive its data one frame time later than the top group to allow for a smooth flow across the boundary between the two groups. The last line of the top group will only start to display its data one line time before the start of the next frame at the top of the display.

This kind of refresh may seem complicated, but it is entirely compatible with the display characteristics for television signals which are generated line by line. Interlacing of fields to form frames may also be accomplished, if required. Thus realistic applications for this micromirror video chip can include television, computer and head-mounted displays.

7. References

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[29] United States Patent 4,229,732 Hartstein, et. al. Oct. 21, 1980 Micromechanical display logic and array Inventors: Hartstein; Allan M. (Chappaqua, NY); Petersen; Kurt E. (San Jose, CA). Assignee: International Business Machines Corporation (Armonk, NY). Appl. No.: 968,054 Filed: Dec. 11, 1978

[30] United States Patent 4,336,536 Kalt, et. al. Jun. 22, 1982 Reflective display and method of making same Inventors: Kalt; Charles G. (29 Hawthorne Rd., Williamstown, MA 01267); Babcock; Bryce (1025 State Rd., North Adams, MA 01247). Appl. No.: 103,995 Filed: Dec. 17, 1979.

[31] United States Patent 4,356,730 Cade Nov. 2, 1982 Electrostatically deformographic switches Inventors: Cade; Paul E. (Colchester, VT). Assignee: International Business Machines Corporation (Armonk, NY). Appl. No.: 223,522 Filed: Jan. 8, 1981.

[32] United States Patent 4,592,628 Altman, et. al. * Jun. 3, 1986 Mirror array light valve Inventors: Altman; Carl (Lagrangeville, NY); Bassous; Ernest (Riverdale, NY); Osburn; Carlton M. (Yorktown Heights, NY); Pleshko; Peter (Staatsburg, NY); Reisman; Arnold (Yorktown Heights, NY); Skolnik; Marvin B. (Kingston, NY). Assignee: International Business Machines (Armonk, NY). [*] Notice: The portion of the term of this patent subsequent to Mar. 3, 2002 has been disclaimed. Appl. No.: 279,392 Filed: Jul. 1, 1981.

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[34] United States Patent 3,981,566 Frank, et. al. Sept. 21, 1976 Lever-action mountings for beam steerer mirrors Inventors: Frank; Lee F. (Rochester, NY); Lee; James K. (Rochester, NY).

Assignee: Eastman Kodak Company (Rochester, NY). Appl. No.: 508,775 Filed: Sept. 23, 1974.

[35] United States Patent 4,203,128 Guckel, et. al. May 13, 1980 Electrostatically deformable thin silicon membranes Inventors: Guckel; Henry (Madison, WI); Larsen; Steven T. (Albany, OR). Assignee: Wisconsin Alumni Research Foundation (Madison, WI). Appl. No.: 944,637 Filed: Sept. 21, 1978

[36] United States Patent 4,013,345 Roach Mar. 22, 1977 Deformable mirror light valve and method of operating the same Inventors: Roach; William Ronald (Rocky Hill, NJ). Assignee: RCA Corporation (New York, NY). Appl. No.: 624,899 Filed: Oct. 22, 1975

[37] United States Patent 4,234,245 Toda, et. al. Nov. 18, 1980 Light control device using a bimorph element Inventors: Toda; Minoru (Machida, JP); Osaka; Susumu (Machida, JP). Assignee: RCA Corporation (New York, NY). Appl. No.: 898,538 Filed: Apr. 20, 1978.

[38] United States Patent 4,210,934 Kutaragi Jul. 1, 1980 Video display apparatus having a flat X-Y matrix display panel Inventors: Kutaragi; Ken (Kawasaki, JP). Assignee: Sony Corporation (Tokyo, JP). Appl. No.: 012,577 Filed: Feb. 15, 1979.

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[48] United States Patent 4,680,579 Ott Jul. 14, 1987 Optical system for projection display using spatial light modulator device Inventors: Ott; Granville E. (Lubbock, TX). Assignee: Texas Instruments Incorporated (Dallas, TX). Appl. No.: 530,327 Filed: Sept. 8, 1983.

[49] United States Patent 4,638,309 Ott Jan. 20, 1987 Spatial light modulator drive system Inventors: Ott; Granville E. (Lubbock, TX). Assignee: Texas Instruments Incorporated (Dallas, TX). Appl. No.: 530,329 Filed: Sept. 8, 1983.

[50] United States Patent 4,710,732 Hornbeck Dec. 1, 1987 Spatial light modulator and method Inventors: Hornbeck; Larry J. (Van Alstyne, TX). Assignee: Texas Instruments Incorporated (Dallas, TX). Appl. No.: 635,966 Filed: Jul. 31, 1984.

[51] United States Patent 4,615,595 Hornbeck Oct. 7, 1986 Frame addressed spatial light modulator Inventors: Hornbeck; Larry J. (Van Alstyne, TX). Assignee: Texas Instruments Incorporated (Dallas, TX). Appl. No.: 659,387 Filed: Oct. 10, 1984.

[52] United States Patent 4,662,746 Hornbeck May 5, 1987 Spatial light modulator and method Inventors: Hornbeck; Larry J. (Van Alstyne, TX). Assignee: Texas Instruments Incorporated (Dallas, TX). Appl. No.: 792,947 Filed: Oct. 30, 1985

[53] United States Patent 4,956,619 Hornbeck Sept. 11, 1990 Spatial light modulator Inventors: Hornbeck; Larry J. (Van Alstyne, TX). Assignee: Texas Instruments Incorporated (Dallas, TX). Appl. No.: 266,220 Filed: Oct. 28, 1988.

[54] United States Patent 4,954,789 Sampsell Sept. 4, 1990 Spatial light modulator Inventors: Sampsell; Jeffrey B. (Plano, TX). Assignee: Texas Instruments Incorporated (Dallas, TX). Appl. No.: 413,924 Filed: Sept. 28, 1989.

[55] United States Patent 5,018,256 Hornbeck May 28, 1991 Architecture and process for integrating DMD with control circuit substrates Inventors: Hornbeck; Larry J. (Van Alstyne, TX). Assignee: Texas Instruments Incorporated (Dallas, TX). Appl. No.: 546,331 Filed: Jun. 29, 1990.

[56] United States Patent 5,083,857 Hornbeck Jan. 28, 1992 Multi-level deformable mirror device Inventors: Hornbeck; Larry J. (Van Alstyne, TX). Assignee: Texas Instruments Incorporated (Dallas, TX). Appl. No.: 546,465 Filed: Jun. 29, 1990.

[57] United States Patent 5,148,157 Florence Sept. 15, 1992 Spatial light modulator with full complex light modulation capability Inventors: Florence; James M. (Richardson, TX). Assignee: Texas Instruments Incorporated (Dallas, TX). Appl. No.: 590,405 Filed: Sept. 28, 1990.

[58] United States Patent 5,061,049 Hornbeck Oct. 29, 1991 Spatial light modulator and method Inventors: Hornbeck; Larry J. (Van Alstyne, TX). Assignee: Texas Instruments Incorporated (Dallas, TX). Appl. No.: 582,804 Filed: Sept. 13, 1990.

[59] United States Patent 5,096,279 Hornbeck, et. al. Mar. 17, 1992 Spatial light modulator and method Inventors: Hornbeck; Larry J. (Van Alstyne, TX); Nelson; William E. (Dallas, TX). Assignee: Texas Instruments Incorporated (Dallas, TX). Appl. No.: 618,013 Filed: Nov. 26, 1990

[60] United States Patent 5,255,100 Urbanus Oct. 19, 1993 Data formatter with orthogonal input/output and spatial reordering Inventors: Urbanus; Paul M. (Dallas, TX). Assignee: Texas Instruments Incorporated (Dallas, TX). Appl. No.: 755,981 Filed: Sept. 6, 1991.

[61] United States Patent 5,285,407 Gale, et. al. Feb. 8, 1994 Memory circuit for spatial light modulator Inventors: Gale; Richard O. (Richardson, TX); Perrone; Benjamin (Dallas, TX). Assignee: Texas Instruments Incorporated (Dallas, TX). Appl. No.: 815,441 Filed: Dec. 31, 1991.

[62] United States Patent 5,285,196 Gale, Jr. Feb. 8, 1994 Bistable DMD addressing method Inventors: Gale, Jr.; Richard O. (Richardson, TX). Assignee: Texas Instruments Incorporated (Dallas, TX). Appl. No.: 961,997 Filed: Oct. 15, 1992

[63] United States Patent 5,280,277 Hornbeck Jan. 18, 1994 Field updated deformable mirror device Inventors: Hornbeck; Larry J. (Van Alstyne, TX). Assignee: Texas Instruments Incorporated (Dallas, TX). Appl. No.: 978,300 Filed: Nov. 17, 1992.

[64] United States Patent 5,212,582 Nelson May 18, 1993 Electrostatically controlled beam steering device and method Inventors: Nelson; William E. (Dallas, TX). Assignee: Texas Instruments Incorporated (Dallas, TX). Appl. No.: 846,305 Filed: Mar. 4, 1992.

[65] United States Patent 5,278,652 Urbanus, et. al. Jan. 11, 1994 DMD architecture and timing for use in a pulse width modulated display system Inventors: Urbanus; Paul M. (Dallas, TX); Sampsell; Jeffrey B. (Plano, TX). Assignee: Texas Instruments Incorporated (Dallas, TX). Appl. No.: 035,525 Filed: Mar. 23, 1993.

[66] United States Patent 5,445,559 Gale, et. al. Aug. 29, 1995 Wafer-like processing after sawing DMDs Inventors: Gale; Richard O. (Richardson, TX); Mignardi; Michael A. (Dallas, TX). Assignee: Texas Instruments Incorporated (Dallas, TX). Appl. No.: 082,183 Filed: Jun. 24, 1993.

[67] United States Patent 5,457,493 Leddy, et. al. Oct. 10, 1995 Digital micro-mirror based image simulation system Inventors: Leddy; Michael (Dallas, TX); Boysel; Mark (Plano, TX); Delong; James A. (Shady Shores, TX); Florence; James M. (Richardson, TX); Lin; Tsen-Hwang (Dallas, TX); Sampsell; Jeffrey (Plano, TX). Assignee: Texas Instruments Incorporated (Dallas, TX). Appl. No.: 121,710 Filed: Sept. 15, 1993.

[68] United States Patent 5,382,961 Gale, Jr. * Jan. 17, 1995 Bistable DMD addressing method Inventors: Gale, Jr.; Richard O. (Richardson, TX). Assignee: Texas Instruments Incorporated (Dallas, TX). [*] Notice: The portion of the term of this patent subsequent to Feb. 8, 2011 has been disclaimed. Appl. No.: 148,127 Filed: Nov. 5, 1993.

[69] United States Patent 5,452,024 Sampsell Sept. 19, 1995 DMD display system Inventors: Sampsell; Jeffrey B. (Plano, TX). Assignee: Texas Instruments Incorporated (Dallas, TX). Appl. No.: 146,385 Filed: Nov. 1, 1993.

[70] United States Patent 5,444,566 Gale, et. al. Aug. 22, 1995 Optimized electronic operation of digital micromirror devices Inventors: Gale; Richard O. (Richardson, TX); Liaison; Randall S. (Plano, TX); Cleveland; Harlan P. (Garland, TX); Chi; Henry (Plano, TX); Davis; Carl W. (Plano, TX); Iambic; Scott D. (Dallas, TX); Few; Claude E. (Dallas, TX). Assignee: Texas Instruments Incorporated (Dallas, TX). Appl. No.: 206,812 Filed: Mar. 7, 1994.

[71] United States Patent 5,331,454 Hornbeck Jul. 19, 1994 Low reset voltage process for DMD Inventors: Hornbeck; Larry J. (Van Alstyne, TX). Assignee: Texas Instruments Incorporated (Dallas, TX). Appl. No.: 823,580 Filed: Jan. 16, 1992.

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[93] United States Patent 4,383,255 Grandjean, et. al. May 10, 1983 Miniature display device Inventors: Grandjean; Pierre-Andre (Neuchatel, CH); Cadman; Martyn-Andrew (Hauterive, CH); Vuilleumier; Raymond (Fontainemelon, CH); Guye; Raymond (Colombier, CH). Assignee: Centre Electronique Horloger S.A. (Neuchatel, CH). Appl. No.: 242,298 Filed: Mar. 10, 1981.

[94] United States Patent 3,979,758 Kilby, et. al. Sept. 7, 1976 Electrostatic head with toner attracting plates Inventors: Kilby; Jack S. (7723 Midbury, Dallas, TX 75230); Lathrop; Jay W. (211 Lark Circle, Clemson, SC 29631). Appl. No.: 542,286 Filed: Jan. 20, 1975

[95] United States Patent 3,989,357 Kalt Nov. 2, 1976 Electrostatic device with rolling electrode Inventors: Kalt; Charles G. (Hawthorne Road, Williamstown, MA 01267). Appl. No.: 580,572 Filed: May 27, 1975.

[96] United States Patent 4,065,677 Micheron, et. al. Dec. 27, 1977 Electrically controlled switching device Inventors: Micheron; Francois (Paris, FR); Doriath; Gerard (Paris, FR); Spitz; Eric (Paris, FR). Assignee: Thomson-CSF (Paris, FR). Appl. No.: 643,645 Filed: Dec. 23, 1975.

[97] United States Patent 4,105,294 Peck Aug. 8, 1978 Electrostatic device Inventors: Peck; David B. (Williamstown, MA). Assignee: Dielectric Systems International, Inc. (Williamstown, MA). Appl. No.: 711,612 Filed: Aug. 4, 1976.

[98] United States Patent 4,163,162 Micheron Jul. 31, 1979 Bistable electret system Inventors: Micheron; Francois (Paris, FR). Assignee: Thomson-CSF (Paris, FR). Appl. No.: 865,330 Filed: Dec. 28, 1977.

[99] United States Patent 4,160,583 Ueda Jul. 10, 1979 Electrostatic display device Inventors: Ueda; Hirotada (Kobe, JP). Assignee: Displaytek Corporation (BOTH OF, JP); Daiwa Shinku Corporation (BOTH OF, JP). Appl. No.: 891,115 Filed: Mar. 28, 1978.

[100]United States Patent 4,229,081 Jones, et. al. Oct. 21, 1980 Electromechanical image converter Inventors: Jones; Terry L. (Springfield, VA); Miller; Brian S. (Alexandria, VA). Assignee: The United States of America as represented by the Secretary of the Army (Washington, DC). Appl. No.: 919,182 Filed: Jun. 26, 1978.

[101]United States Patent 4,494,826 Smith Jan. 22, 1985 Surface deformation image device Inventors: Smith; James L. (426 High School Dr., Grand Prairie, TX 75050). Appl. No.: 108,933 Filed: Dec. 31, 1979.

[102]United States Patent 4,564,836 Vuilleumier, et. al. Jan. 14, 1986 Miniature shutter type display device with multiplexing capability Inventors: Vuilleumier; Raymond (Fontainemelon, CH); Weiss; Paul-Charles (Neuchatel, CH). Assignee: Centre Electronique Horloger S.A. (Neuchatel, CH). Appl. No.: 392,073 Filed: Jun. 25, 1982.

[103]United States Patent 4,454,547 Yip, et. al. Jun. 12, 1984 Raster output scanner having a full width electromechanical modulator Inventors: Yip; Kwok L. (Webster, NY); Hsing; To R. (Sudbury, MA); Daniele; Joseph J. (Pittsford, NY); Ritter; Joachim A. (Webster, NY). Assignee: Xerox Corporation (Stamford, CT). Appl. No.: 394,603 Filed: Jul. 2, 1982

[104]United States Patent 4,492,435 Banton, et. al. Jan. 8, 1985 Multiple array full width electromechanical modulator Inventors: Banton; Martin E. (Fairport, NY); Lavallee; Pierre A. (Penfield, NY); Araghi; Mehdi N. (West Webster, NY); Daniele; Joseph J. (Pittsford, NY); Yip; Kwok L. (Webster, NY). Assignee: Xerox Corporation (Stamford, CT). Appl. No.: 394,604 Filed: Jul. 2, 1982.

[105]United States Patent 4,725,832 Lorteije, et. al. Feb. 16, 1988 Electroscopic picture display arrangement Inventors: Lorteije; Jean H. J. (Eindhoven, NL); Te Velde; Ties S. (Eindhoven, NL); De Leeuw; Henricus F. A. (Eindhoven, NL); Stroomer; Martinus V. C. (Eindhoven, NL); Kuijk; Karel E. (Eindhoven, NL). Assignee: U.S. Philips Corporation (New York, NY). Appl. No.: 746,211 Filed: Jun. 18, 1985.

[106]United States Patent 4,709,995 Kuribayashi, et. al. Dec. 1, 1987 Ferroelectric display panel and driving method therefor to achieve gray scale Inventors: Kuribayashi; Masaki (Higashikurume, JP); Nakazawa; Toshihiko (Yokohama, JP); Kanbe; Junichiro (Yokohama, JP). Assignee: Canon Kabushiki Kaisha (Tokyo, JP). Appl. No.: 763,432 Filed: Aug. 7, 1985.

[107]United States Patent 4,842,396 Minoura, et. al. Jun. 27, 1989 Light modulation element and light modulation apparatus Inventors: Minoura; Kazuo (Yokohama, JP); Matsuoka; Kazuhiko (Yokohama, JP). Assignee: Canon Kabushiki Kaisha (Tokyo, JP). Appl. No.: 748,835 Filed: Jun. 26, 1985.

[108]United States Patent 4,698,602 Armitage Oct. 6, 1987 Micromirror spatial light modulator Inventors: Armitage; David (Los Altos, CA). Assignee: The United States of America as represented by the Secretary of the Air Force (Washington, DC). Appl. No.: 785,691 Filed: Oct. 9, 1985.

[109]United States Patent 4,755,013 Setani Jul. 5, 1988 Light scanning optical system of an image output scanner using an electromechanical light modulator Inventors: Setani; Michitaka

(Kawasaki, JP). Assignee: Canon Kabushiki Kaisha (Tokyo, JP). Appl. No.: 115,564 Filed: Oct. 29, 1987.

[110] United States Patent 4,793,699 Tokuhara Dec. 27, 1988 Projection apparatus provided with an electromechanical transducer element Inventors: Tokuhara; Mitsuhiro (Chigasaki, JP). Assignee: Canon Kabushiki Kaisha (Tokyo, JP). Appl. No.: 180,618 Filed: Apr. 4, 1988.

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Appendix A. Berkeley Process Flow

All deposition times and etch times are approximate and should be calculated for current rates.

Process Steps

0. Preparation
   - 0.1 Number all wafers
   - 0.2 Profile base flatness for film stress using Flexus

0. Grow oxide [include test wafer (tw1)[1]]
   - 0.1 Wafer clean - include hydrofluoric acid (hf) dip
   - 0.2 Swetoxb recipe time =2 hr temp = 1000°C Tox =5000Å
   - 0.3 Measure the film thickness on nanospec
   - 0.4 Wet etch oxide off of the back of test wafer 1 (be sure to use at least two coats of photo resist for all wet etches - pinholes will destroy devices)
   - 0.5 Measure film stress on test wafer 1.

0. Deposit polysilicon for column conductors [include pcw[2] 1]
   - 0.1 Wafer clean
   - 0.2 16dvplya recipe time =6hr 40min thickness 10000Å
   - 0.3 Rapid Thermal Anneal (RTA) Heatpulse 900°C 1min
   - 0.4 Nanospec pcw1
   - 0.5 Etch backside pcw1
   - 0.6 Measure film stress
   - 0.7 Measure film resistivity
   - 0.8 Pattern the column conductors (mask: CPG emul[3] cf[4])
     - 0.8.1 Photo module
       - 0.8.1.1 HMDS prime in prime oven
       - 0.8.1.2 Spin on i-line photoresist using svgcoat 1or 2. Apply multiple layers to achieve required thickness. Resist used is Olin 10i spinspeed is 0000 for 1 nominal and 0000 for 1.5 nominal thickness. Bake for 60sec at 90°C.
       - 0.8.1.3 Expose using selected mask in GCA wafer stepper. Be sure to use aperatures on clear-field masks.
       - 0.8.1.4 Post-exposure bake using svgdev 1 min 120°C
       - 0.8.1.5 Develop using svgdev. 1 minute Olin xxxx
       - 0.8.1.6 Optical microscope inspect for alignment/resolution/scum - in case of failed inspection, strip PR in PRS3000 and restart

1. tw - test wafer #
2. pcw- polycontrol wafer - has 1000Å of thermal oxide over bulk silicon
3. emulsion
4. cf - clear field; df - dark field

photo module.
0.8.1.7 Descum in Technics-C
0.8.1.8 Optical inspection
0.8.1.9 Hard-Bake in oven 120°C for 30 min. (required on some mask layers to improve etch selectivity.)
0.8.2 Lam 5 etch recipe: 5003 etch rate : ~4000A/m time: 280
0.8.3 Probe for open at process control square 1 (sq 1) all wafers!
0.8.4 Strip photoresist oxygen plasma Technics-C.
0.8.5 Remove photomask in PRS3000 spindrier
0.8.6 Measure residual film thickness
0.9 Profile

0. LPCVD LTO [tw1][1] 3.5µm 3.5hr dep time (due to nonuniformity of this deposition, do two runs with 180° rotation of the wafers between runs)
0.1 Measure total oxide thickness
0.2 Profile
0.3 CMP down to poly [include tw1]
0.4 Profile — should be flat
0.5 Densify using PSGDENS 900°C 1hr.
0.6 Etch off backside of test wafer 1
0.7 Measure film stress
0.8 Measure total oxide thickness
0.9 Profile
0.10 Pattern oxide die edges (mask: MECH chrome df)[tw1]
0.11 Nanospec for complete removal
0.12 Remove photomask
0.13 Profile trenches

0. Nitride deposition [test wafer 1&2]
0.1 Deposit 1500A low stress nitride
Recipe: BSLOWI Deposition time: 30 min
0.2 Anneal 900°C 1 hr
0.3 Measure thickness
0.4 Etch off backside of tw2
0.5 Measure stress
0.6 Pattern contact holes through nitride and glass [test wafer 1&2]
0.6.1 Photo module (mask: NITR chrome df)
0.6.2 Lam 2 nitride/oxide etch
0.6.3 Remove photomask
0.7 Measure process control squares

0. Polysilicon [pcw 2]
0.1 Wafer clean including hf dip
0.2 Deposit poly recipe: 16doplya 8000Å deposition time: 400min temp: std (if fabbing high electrodes double deposition time)

1. Include [wafer]

0.3 Anneal 900°C 1 min
0.4 Measure resistivity on pcw2
0.5 Measure film thickness
0.6 Etch off poly from back of pcw2
0.7 Measure film stress pcw2
0.8 Skip to 8. (for simpler devices without high electrodes)
0.9 Pattern high electrodes (mask: SP1A emul cf)
    0.9.1 Photo module
    0.9.2 Lam 5
    0.9.3 Measure for remaining film thickness
0.10 Probe fuse 1 for contact resistance

0. Deposit nitride insulator layer [test wafer 3] (optional)
    0.1 Anneal
    0.2 Measure thickness
    0.3 Etch off back side of test wafer 3
    0.4 Measure film stress
    0.5 Measure breakdown voltage (optional)
        0.5.1 Metalize front side tw3
        0.5.2 Photo pattern squares on front of tw3(mask: MECH reuse!)
        0.5.3 Measure breakdown voltage
    0.6 Pattern nitride (mask: BUMP emul cf)
    0.7 Measure residual film thickness {0}
    0.8 Probe for conductivity sq1
0. Pattern low electrodes (mask: SP1 emul cf)
    0.1 Photo module
    0.2 Measure residual film
    0.3 Probe open sq 1
    0.4 Probe contact resistance fuse 1
    0.5 Profile
0. Deposit LTO 40000Å 4hr [test wafer 4]
    0.1 Anneal
    0.2 Measure film thickness
    0.3 Profile
0. Chemical Mechanical Polish down to Poly in the array!
    0.1 Measure film thickness
    0.2 Profile {flat!}
    0.3 Deposit 13700Å LTO (controls spring height)
0. Pattern posts (mask: PSG1 chrome df)
    0.1 Probe for contact on fuse 1
0. Polysilicon posts [pcw4]
    0.1 Wafer clean with hf dip
    0.2 Deposit poly 10000Å recipe: 16LOPH3A deposition time: 160 min temp: 590°
        flows: SIH4: 100 PH3: 10 pressure: 2500 mTorr
    0.3 Anneal : none!

0.4 Measure film thickness
0.5 Measure resistance
0.6 Etch off backside of pcw4
0.7 Measure stress pcw4
0.8 Photo step for yokes(mask: SP2A)
0.9 Etch poly
0.10 Probe resistance fuse2
0.11 Profile posts and yoke

0. Pattern ditches for vertical springs
   0.1 Photo module (mask PSG4 chrome df)
   0.2 Etch oxide Lam2 recipe: time:
   0.3 Strip resist
0. Ultra thin poly [pcw 5,6,7]
   0.1 Wafer clean with hf dip
   0.2 Next three depositions are all recipe: 16LOPH3A temp: 590°
   flows: SIH4: 100 PH3: 10 pressure: 2500 mTorr
   0.3 Deposit poly on wafers 1-4 pcw5 900Å deposition time: 13.5 min
   0.4 Deposit poly on wafers 5-7 pcw6 1000Å deposition time: 16 min
   0.5 Deposit poly on wafers 8-10 pcw7 1500Å deposition time: 24 min
   0.6 Anneal RTA 900° 60s
   0.7 Measure film thicknesses pcw 5,6,7
   0.8 Measure resistance pcw 5,6,7
   0.9 Etch off backside of pcw 5,6,7
   0.10 Measure stress pcw 5,6,7
   0.11 Pattern torsion hinges and posts
      0.11.1 Photo module (mask: SP2 emul cf)
      0.11.2 Etch lam 5 recipe: time:
      0.11.3 Measure residual film thickness {0}
   0.12 Probe resistance fuse3 and 2
0. Deposit LTO 14000Å 1.4 hrs[test wafer 5]
   0.1 Anneal 650° 1 hr
   0.2 Pattern the mirror standoffs [tw 5 - probe for contact]
      0.2.1 Photo module (mask: PSG2 chrome df)
   0.3 Probe fuses 4,5
0. Polysilicon mirrors and mirror standoffs [pcw8]
   0.1 Wafer clean including hf dip
   0.2 Deposit poly 5000Å recipe: 16LOPH3A deposition time: 80 min temp: 590
   flows: SIH4: 100 PH3: 10 pressure: 2500 mTorr
   0.3 Anneal: no
   0.4 Measure film thickness
   0.5 Etch off backside of pcw3
   0.6 Measure stress pcw3
   0.7 Remove all backside depositions (This is only to allow ground contact to be made from the package to the substrate). This can be wet etches or sent out for

grinding. With wet etches protect the front side with at least two coats of P.R.
- 0.7.1 Poly
- 0.7.2 LTO
- 0.7.3 Poly
- 0.7.4 LTO
- 0.7.5 Poly
- 0.7.6 Nitride
- 0.7.7 LTO
- 0.7.8 Poly
- 0.7.9 Oxide

0.8 CMP the surface to mirror finish [pcw8]
0.9 Measure film thickness
0.10 Measure reflectance

0. Sputter or evaporate on a thin gold or aluminum reflective coating
   - 0.1 Measure reflectance
   - 0.2 Plasma etch to pattern mirrors Al & Poly
     - 0.2.1 Photo module (mask:SP3 emul cf)
     - 0.2.2 Plasma etch
     - 0.2.3 Don’t remove photmask!
   - 0.3 Probe open fuse 6
   - 0.4 Probe contact resistance fuse 7
0. Dicing
   - 0.1 Spin on a protective layer of photoresist
   - 0.2 Apply dicing adhesive film to hoop and center the wafer onto the film. Remove air bubbles using rubber roller.
   - 0.3 Dice using Disco saw.
0. Release and dry
   - 0.1 Place 1 or 2 individual die into specially designed teflon carrier
   - 0.2 Release
     - 0.2.1 Place the teflon carrier in a 50ml teflon beaker.
     - 0.2.2 Soak in for 5 min. with frequent agitation.
     - 0.2.3 Aspirate the acetone and rinse thoroughly.
     - 0.2.4 Release etch 49% HF for 15 minutes (in the DARK if aluminum coated to prevent damage to aluminum)
     - 0.2.5 Exchange rinse with water
   - 0.3 Optional SAM coat (see recipe)
   - 0.4 Exchange rinse with isopropanol and then methanol
   - 0.5 Critical point CO_2 dry (still in teflon carrier)

Table A.1 Wafer variations

Wafer	Spring thickness Å
1	900
2	900
3	900
4	900
5	1000
6	1000
7	1000
8	1000
9	1500
10	1500
11	1500
12	1500

Appendix B. Berkeley Process Recipes

To allow duplication of this process at another site, the details of the recipes that are in use at the Berkeley Microfabrication Laboratory at this time are provided here. These recipes are the work of others, with the exception of the CMP recipe. Special times or other parameters that are required by these recipes are provided in the detailed process flow in Appendix A.

B.1 CVD

These recipes are run on Tylan or Tystar furnaces.

Doped Polysilicon

```
process id: 16doplyb
description:  doped  poly  post  mfc
              change  to  1-10sccm
              (parsa,apr9
bank: 1
tubes: 16
reuse: yes

0001.0000     STEP ready
0001.0005        dtcena=on
0001.0010        n2=on
0001.0015        n2=5000
0001.0020        templ=variable (std
                 loading temp 604)
0001.0025        tempc=variable (std
                 loading temp 610)
0001.0030        temps=variable (std
                 loading temp 616)
0001.0035        kr=30
0001.0040        kc=15
0001.0045        kp=24
0001.0050        templ tolerance=3
0001.0055        tempc tolerance=2
0001.0060        temps tolerance=3
0001.0065        mtorr tolerance=80
0001.0070        sih4 tolerance=10
0001.0075        ph3 tolerance=0.5
0001.0080        vacuum=off
0001.0085        sih4=off
0001.0090        sih4=0.0
0001.0095        ph3=off
0001.0100        ph3=0.0
0001.0105        kxlc=4
0001.0110        kxcc=3
0001.0115        kxsc=4
0001.0120        kxlh=50
0001.0125        kxsh=50

0005.0000     STEP unload
0005.0005        time:00:05:00
0005.0010        unload=on
0005.0015          if bpout=on goto
                 0010
0005.0020          if almack=on goto
                 0015

0010.0000     STEP load hold
0010.0005        time:00:30:00
0010.0010          if almack=on goto
                 0015
0010.0015        unload=off

0015.0000     STEP load
0015.0005        time:00:00:00
0015.0010        unload=off
0015.0015        load=on
0015.0020          if dntlk=on goto
                 0020
0015.0025          if almack=on goto
                 0020

0020.0000     STEP short wait
0020.0005        time:00:00:20
0020.0010        load=on
0020.0015        n2=100
0020.0020          if dntlk=off goto
                 0105

0025.0000     STEP short pump
0025.0005        time:00:01:00
0025.0010        vacuum=on
0025.0015        n2=100
0025.0020        templ=variable (std
                 dep temp 604)
0025.0025        tempc=variable (std
                 dep temp 610)
0025.0030        temps=variable (std
                 dep temp 616)
0025.0035          if almack=on goto
                 0030
0025.0040          if vntlk=off goto
                 0095
0025.0045        load=off

0030.0000     STEP temp stabiliza-
```

```
              tion
0030.0005       time:00:01:00
0030.0010       vacuum=on
0030.0015        if almack=on goto
              0040
0030.0020       load=off
0030.0025        if mtorr>4800 goto
              0095

0035.0000    STEP step temp check
0035.0005       time:00:03:00
0035.0010        if templ#variable
              goto 0030 (same as
              dep templ)
0035.0015        if tempc#variable
              goto 0030 (same as
              dep tempc)
0035.0020        if temps#variable
              goto 0030 (same as
              dep temps)
0035.0025       if mtorr>4800 goto
              0095

0040.0000    STEP pumpdown
0040.0005       time:00:02:00
0040.0010       n2=off
0040.0015       n2=0
0040.0020       vacuum=on
0040.0025        if almack=on goto
              0045
0040.0030        if mtorr>4800 goto
              0095

0045.0000    STEP leaktest
0045.0005       time:00:01:00
0045.0010       vacuum=off
0045.0015        if mtorr>250 goto
              0095
0045.0020        if almack=on goto
              0050

0050.0000    STEP sih4
0050.0005       time:00:00:30
0050.0010       sih4=on
0050.0015       sih4=100
0050.0020       vacuum=on
0050.0025        if almack=on goto
              0055

0055.0000    STEP phosphine
0055.0005       time:00:00:30
0055.0010       ph3=on
0055.0015       ph3=2.0
0055.0020       vacuum=on
0055.0025        if almack=on goto
              0060

0060.0000    STEP specify pressure
0060.0005       time:00:00:30
0060.0010         mtorr=on turn on
              pressure control
0060.0015       mtorr=1875 (375 mt
              times 5 - new scale)
0065.0000        STEP let pressure/
              silane to stabilize
0065.0005        time:00:01:00
0065.0010        if mtorr>4800 goto
              0095
0065.0015        if almack=on goto
              0070

0070.0000    STEP deposition
0070.0005       time:variable poly
              dep time
0070.0010       if mtorr>4800 goto
              0095
0070.0015        if almack=on goto
              0075

0075.0000    STEP pump
0075.0005       time:00:03:00
0075.0010       sih4=0
0075.0015       sih4=off
0075.0020       ph3=0
0075.0025       ph3=off
0075.0030        mtorr=off turn off
              pressure control
0075.0035         mtorr=0 turn off
              pressure control
0075.0040       vacuum=on

0080.0000    STEP pre-flush
0080.0005       time:00:00:30
0080.0010       vacuum=on
0080.0015       n2=on
0080.0020       n2=100
0080.0025       ph3=0
0080.0030       ph3=off
0080.0035       sih4=off
0080.0040       sih4=0

0085.0000    STEP flush (n2 + vac)
0085.0005       time:00:15:00
0085.0010       vacuum=on
0085.0015       n2=on
0085.0020       n2=100
0085.0025       ph3=0
0085.0030       ph3=off
0085.0035       sih4=off
0085.0040       sih4=0
0085.0045        if mtorr>4800 goto
              0095

0090.0000    STEP hold until ack
0090.0005       time:00:00:00
0090.0010        if almack=on goto
              0095

0095.0000    STEP back fill #1
0095.0005       time:00:05:00
0095.0010       vacuum=off
0095.0015       n2=on
0095.0020       n2=ramp to 5000
```

```
                                        0100.0020       n2=5000
0100.0000    STEP back fill # 2
0100.0005       time:00:05:00           0105.0000    STEP
0100.0010       vacuum=off              0105.0005       end process
0100.0015       n2=on
```

Doped Amourphous Silicon (run at 590°C)

```
process id: 16loph3a                    0015.0015       load=on
description:  alt  ph3  cyl  lo  flow   0015.0020         if dntlk=on goto
              doped  ply  (11/21/96                      0020
              jfk)                      0015.0025        if almack=on goto
bank: 1                                                  0020
tubes: 16
reuse: yes                              0020.0000    STEP short wait
                                        0020.0005       time:00:00:20
0001.0000    STEP ready                 0020.0010       load=on
0001.0005       dtcena=on               0020.0015       n2=100
0001.0010       n2=on                   0020.0020        if dntlk=off goto
0001.0015       n2=5000                                  0105
0001.0020       templ=600
0001.0025       tempc=600               0025.0000    STEP short pump
0001.0030       temps=600               0025.0005       time:00:01:00
0001.0035       kr=30                   0025.0010       vacuum=on
0001.0040       kc=15                   0025.0015       n2=100
0001.0045       kp=24                   0025.0020       templ=variable
0001.0050       templ tolerance=3       0025.0025       tempc=variable
0001.0055       tempc tolerance=2       0025.0030       temps=variable
0001.0060       temps tolerance=3       0025.0035        if almack=on goto
0001.0065       mtorr tolerance=80                       0030
0001.0070       sih4 tolerance=10       0025.0040        if vntlk=off goto
0001.0075       ph3 tolerance=0.5                        0095
0001.0080       vacuum=off              0025.0045       load=off
0001.0085       sih4=off
0001.0090       sih4=0.0                0030.0000     STEP temp stabiliza-
0001.0095       ph3=off                                  tion
0001.0100       ph3=0.0                 0030.0005       time:00:01:00
0001.0105       kxlc=4                  0030.0010       vacuum=on
0001.0110       kxcc=3                  0030.0015        if almack=on goto
0001.0115       kxsc=4                                   0040
0001.0120       kxlh=50                 0030.0020       load=off
0001.0125       kxsh=50                 0030.0025        if mtorr>4800 goto
                                                         0095
0005.0000    STEP unload
0005.0005       time:00:05:00           0035.0000    STEP step temp check
0005.0010       unload=on               0035.0005       time:00:03:00
0005.0015         if bpout=on goto      0035.0010        if templ#variable
                  0010                                   goto 0030
0005.0020         if almack=on goto     0035.0015        if tempc#variable
                  0015                                   goto 0030
                                        0035.0020        if temps#variable
0010.0000    STEP load hold                             goto 0030
0010.0005       time:00:30:00           0035.0025       if mtorr>4800 goto
0010.0010        if almack=on goto                      0095
                 0015
0010.0015       unload=off              0040.0000    STEP pumpdown
                                        0040.0005       time:00:02:00
0015.0000    STEP load                  0040.0010       n2=off
0015.0005       time:00:00:00           0040.0015       n2=0
0015.0010       unload=off              0040.0020       vacuum=on
```

```
0040.0025        if almack=on goto
                 0045
0040.0030        if mtorr>4800 goto
                 0095

0045.0000    STEP leaktest
0045.0005       time:00:01:00
0045.0010       vacuum=off
0045.0015        if mtorr>250 goto
                 0095
0045.0020        if almack=on goto
                 0050

0050.0000    STEP specify sih4
0050.0005       time:00:00:30
0050.0010       sih4=on
0050.0015          sih4=variable 6
                 sccm minimum or ph3
                 wont flow
0050.0020        if almack=on goto
                 0055
0050.0025       vacuum=on

0055.0000    STEP phosphine
0055.0005       time:00:00:30
0055.0010        anao4=on switch to
                 alternate gas cylin-
                 der
0055.0015       ph3=on
0055.0020        ph3=variable 0-10
                 sccm  1.6%  ph3  in
                 silane
0055.0025       vacuum=on
0055.0030        if almack=on goto
                 0060

0060.0000    STEP specify pressure
0060.0005       time:00:00:30
0060.0010         mtorr=on turn on
                 pressure control
0060.0015              mtorr=variable
                 enter value times 5

0065.0000      STEP  let  pressure/
                 silane to stabilize
0065.0005       time:00:01:00
0065.0010        if mtorr>4800 goto
                 0095
0065.0015        if almack=on goto
                 0070

0070.0000    STEP deposition
0070.0005       time:variable poly
                 dep time
0070.0010        if mtorr>4800 goto
                 0095
0070.0015        if almack=on goto
                 0075

0075.0000    STEP pump
0075.0005       time:00:03:00
0075.0010       sih4=0
0075.0015       sih4=off
0075.0020       ph3=0
0075.0025       ph3=off
0075.0030          anao4=off switch
                 back to std ph3 cyl-
                 inder
0075.0035        mtorr=off turn off
                 pressure control
0075.0040           mtorr=0 turn off
                 pressure control
0075.0045       vacuum=on

0080.0000    STEP pre-flush
0080.0005       time:00:00:30
0080.0010       vacuum=on
0080.0015       n2=on
0080.0020       n2=100
0080.0025       ph3=0
0080.0030       ph3=off
0080.0035       sih4=off
0080.0040       sih4=0

0085.0000    STEP flush (n2 + vac)
0085.0005       time:00:15:00
0085.0010       vacuum=on
0085.0015       n2=on
0085.0020       n2=100
0085.0025       ph3=0
0085.0030       ph3=off
0085.0035       sih4=off
0085.0040       sih4=0
0085.0045        if mtorr>4800 goto
                 0095

0090.0000    STEP hold until ack
0090.0005       time:00:00:00
0090.0010        if almack=on goto
                 0095

0095.0000    STEP back fill #1
0095.0005       time:00:05:00
0095.0010       vacuum=off
0095.0015       n2=on
0095.0020       n2=ramp to 5000
0095.0025       ph3=0
0095.0030       ph3=off
0095.0035       sih4=0
0095.0040       sih4=off

0100.0000    STEP back fill #2
0100.0005       time:00:05:00
0100.0010       vacuum=off
0100.0015       n2=on
0100.0020       n2=5000

0105.0000    STEP
0105.0005       end process
```

Low Stress Silicon Nitride

```
BSLOWI.018
IDLE CONDITION
STEP: IDLE    COMMENT: IDLE STATE
    BOATSPD = 25.0 IPM
      TEMPL = 750.0 DEGC
     TEMPLC = 750.0 DEGC
      TEMPC = 750.0 DEGC
     TEMPSC = 750.0 DEGC
     TCUENA = ON
         N2 = 5000. SCCM
      TEMPS = 750.0 DEGC
PROCESS RUN SEQUENCE
STEP: STRT    COMMENT: UNLOAD BOAT
              TIME: 00.03.00
  If  EVENT = ON then goto 0015
         N2 = 5000. SCCM
      TEMPL = 650.0 DEGC
     TEMPLC = 700.0 DEGC
      TEMPC = 700.0 DEGC
     TCUENA = ON
    BOATOUT = ON
    BOATSPD = 25.0 IPM
  If OUTLMT = ON then goto 0010
     TEMPSC = 700.0 DEGC
      TEMPS = 700.0 DEGC
STEP: 0010    COMMENT: LOAD SONIC
              TIME: 00.00.05
      SONIC = ON
         N2 = 5000. SCCM
      TEMPL = 650.0 DEGC
     TEMPLC = 700.0 DEGC
      TEMPC = 700.0 DEGC
  If  EVENT = ON then goto 0015
     TCUENA = ON
     TEMPSC = 700.0 DEGC
      TEMPS = 700.0 DEGC
STEP: 0015    COMMENT: LOAD ON
              EVENTTIME: 00.20.00
  If  EVENT = ON then goto BTIN
     TCUENA = ON
         N2 = 5000. SCCM
      TEMPL = 650.0 DEGC
     TEMPLC = 700.0 DEGC
      TEMPC = 700.0 DEGC
     TEMPSC = 700.0 DEGC
      TEMPS = 700.0 DEGC
STEP: BTIN    COMMENT: BOAT IN FAST
              TIME: 00.03.00
    BOATSPD = 25.0 IPM
  If  INLMT = ON then goto 0025
     TCUENA = ON
     BOATIN = ON
      TEMPL = 650.0 DEGC
         N2 = 5000. SCCM
     TEMPLC = 700.0 DEGC
      TEMPC = 700.0 DEGC
     TEMPSC = 700.0 DEGC
      TEMPS = 700.0 DEGC
STEP: 0025    COMMENT: BOAT IN SLOW
              TIME: 00.02.00
    BOATSPD = 5.0 IPM
      TEMPL = 835.0 DEGC
     TEMPLC = 835.0 DEGC
      TEMPC = 835.0 DEGC
     TEMPSC = 835.0 DEGC
     BOATIN = ON
     TCUENA = ON
         N2 = 5000. SCCM
  If  DNTLK = OFF then goto 0030
      TEMPS = 835.0 DEGC
STEP: 0030    COMMENT: PREDP PUMP 1
              TIME: 00.05.00
      TEMPL = 835.0 DEGC
     TEMPLC = 835.0 DEGC
      TEMPC = 835.0 DEGC
     TEMPSC = 835.0 DEGC
      TEMPS = 835.0 DEGC
     TCUENA = ON
       GATE = ON
  If  PRCPR < 200. MTOR then goto
              0035
STEP: 0035    COMMENT: PREDP PURG 1
              TIME: 00.02.00
      TEMPL = 835.0 DEGC
     TEMPLC = 835.0 DEGC
      TEMPC = 835.0 DEGC
     TEMPSC = 835.0 DEGC
     TCUENA = ON
         N2 = 500. SCCM
       GATE = ON
      TEMPS = 835.0 DEGC
STEP: 0040    COMMENT: PREDP PUMP 2
              TIME: 00.02.00
       GATE = ON
     TCUENA = ON
      TEMPL = 835.0 DEGC
     TEMPLC = 835.0 DEGC
      TEMPC = 835.0 DEGC
     TEMPSC = 835.0 DEGC
      TEMPS = 835.0 DEGC
  If  PRCPR > 1800. MTOR then goto
              ABRT
STEP: 0045    COMMENT: PREDEP
              PURGE 2TIME:
              00.02.00
       GATE = ON
     TCUENA = ON
      TEMPL = 835.0 DEGC
     TEMPLC = 835.0 DEGC
      TEMPC = 835.0 DEGC
         N2 = 500. SCCM
     TEMPSC = 835.0 DEGC
      TEMPS = 835.0 DEGC
STEP: 0050    COMMENT: PREDP PUMP 3
              TIME: 00.02.00
       GATE = ON
```

```
     TCUENA = ON
      TEMPL = 835.0 DEGC
     TEMPLC = 835.0 DEGC
      TEMPC = 835.0 DEGC
     TEMPSC = 835.0 DEGC
      TEMPS = 835.0 DEGC
  If  PRCPR > 1800. MTOR then goto
              ABRT
STEP: 0055    COMMENT: LEAK CHECK
              TIME: 00.01.00
      TEMPL = 835.0 DEGC
     TEMPLC = 835.0 DEGC
      TEMPC = 835.0 DEGC
     TEMPSC = 835.0 DEGC
      TEMPS = 835.0 DEGC
     TCUENA = ON
  If  PRCPR > 100. MTOR then goto
              ABRT
STEP: 0060    COMMENT: TEMP STABI-
              LIZETIME: 00.10.00
     TCUENA = ON
  If TUBEOT = ON then goto ABRT
      TEMPL = 835.0 DEGC
     TEMPLC = 835.0 DEGC
  If  SCROT = ON then goto ABRT
         N2 = 500. SCCM
       GATE = ON
  If TEMPSC out-of-tolerance then
              goto 0060 (NO TOLER-
              ANCE ALARM)
  If  TEMPS out-of-tolerance then
              goto 0060 (NO TOLER-
              ANCE ALARM)
      TEMPC = 835.0 DEGC
     TEMPSC = 835.0 DEGC
      TEMPS = 835.0 DEGC
  If  CABOT = ON then goto ABRT
  If  TEMPL out-of-tolerance then
              goto 0060 (NO TOLER-
              ANCE ALARM)
  If TEMPLC out-of-tolerance then
              goto 0060 (NO TOLER-
              ANCE ALARM)
  If  TEMPC out-of-tolerance then
              goto 0060 (NO TOLER-
              ANCE ALARM)
  If  DNTLK = ON then goto ABRT
  If  GNTLK = ON then goto ABRT
STEP: 0065    COMMENT: PREDEP PUMP
              4TIME: 00.02.00
     TCUENA = ON
       GATE = ON
      TEMPL = 835.0 DEGC
     TEMPLC = 835.0 DEGC
      TEMPC = 835.0 DEGC
     TEMPSC = 835.0 DEGC
      TEMPS = 835.0 DEGC
  If  PRCPR > 1800. MTOR then goto
              ABRT
STEP: 0100    COMMENT: NH3 STABI-
              LIZETIME: 00.01.00
      PRCPR = 140. MTOR
     TCUENA = ON
       GATE = ON
        NH3 = 25.0 SCCM
      PRCPR = 140. MTOR
     TCUENA = ON
       GATE = ON
        NH3 = 25.0 SCCM
      TEMPL = 835.0 DEGC
     TEMPLC = 835.0 DEGC
      TEMPC = 835.0 DEGC
     TEMPSC = 835.0 DEGC
      TEMPS = 835.0 DEGC
STEP: 0105    COMMENT: NH3 FLOW
              TIME: 00.01.00
      PRCPR = 140. MTOR
     TCUENA = ON
       GATE = ON
        NH3 = 25.0 SCCM
      PRCPR = 140. MTOR
     TCUENA = ON
       GATE = ON
        NH3 = 25.0 SCCM
      TEMPL = 835.0 DEGC
     TEMPLC = 835.0 DEGC
      TEMPC = 835.0 DEGC
  If    NH3 out-of-tolerance then
              goto ABRT
     TEMPSC = 835.0 DEGC
      TEMPS = 835.0 DEGC
  If  PRCPR out-of-tolerance then
              goto ABRT
  If TEMPLC out-of-tolerance then
              goto ABRT
  If  TEMPC out-of-tolerance then
              goto ABRT
  If TEMPSC out-of-tolerance then
              goto ABRT
  If TUBEOT = ON then goto ABRT
  If  SCROT = ON then goto ABRT
  If  CABOT = ON then goto ABRT
  If  DNTLK = ON then goto ABRT
  If  GNTLK = ON then goto ABRT
  If  ANTLK = ON then goto ABRT
  If  BNTLK = ON then goto ABRT
  If  VNTLK = ON then goto ABRT
STEP: 0110    COMMENT: GAS STABI-
              LIZETIME. 00.01.00
      PRCPR = 140. MTOR
     TCUENA = ON
       GATE = ON
        NH3 = 25.0 SCCM
      PRCPR = 140. MTOR
     TCUENA = ON
       GATE = ON
        NH3 = 25.0 SCCM
      TEMPL = 835.0 DEGC
     TEMPLC = 835.0 DEGC
      TEMPC = 835.0 DEGC
     TEMPSC = 835.0 DEGC
      TEMPS = 835.0 DEGC
        DCS = 100.0 SCCM
```

```
STEP: 0115    COMMENT: DEPOSITION
              TIME: variable/
              00.00.00
  If  VNTLK = ON then goto ABRT
  If  GNTLK = ON then goto ABRT
  If TUBEOT = ON then goto ABRT
  If  SCROT = ON then goto ABRT
      TEMPS = 835.0 DEGC
     TCUENA = ON
       GATE = ON
        DCS = 100.0 SCCM
  If    DCS out-of-tolerance then
              goto ABRT
        NH3 = 25.0 SCCM
  If  PRCPR out-of-tolerance then
              goto ABRT
  If TEMPLC out-of-tolerance then
              goto ABRT
      PRCPR = 140. MTOR
  If  CABOT = ON then goto ABRT
  If    NH3 out-of-tolerance then
              goto ABRT
  If  TEMPC out-of-tolerance then
              goto ABRT
  If TEMPSC out-of-tolerance then
              goto ABRT
  If  DNTLK = ON then goto ABRT
  If  ANTLK = ON then goto ABRT
  If  PRCPR > 1800. MTOR then goto
              ABRT
  If  BNTLK = ON then goto ABRT
      TEMPL = 835.0 DEGC
     TEMPLC = 835.0 DEGC
      TEMPC = 835.0 DEGC
     TEMPSC = 835.0 DEGC
STEP: 0120    COMMENT: GAS STABI-
              LIZETIME: 00.01.00
      TEMPS = 835.0 DEGC
     TCUENA = ON
       GATE = ON
        NH3 = 95.0 SCCM
      PRCPR = 140. MTOR
      TEMPL = 835.0 DEGC
     TEMPLC = 835.0 DEGC
      TEMPC = 835.0 DEGC
     TEMPSC = 835.0 DEGC
STEP: 0125    COMMENT: ETC CONDI-
              TIONTIME: 00.15.00
      TEMPL = 835.0 DEGC
     TEMPLC = 835.0 DEGC
      TEMPC = 835.0 DEGC
     TEMPSC = 835.0 DEGC
      TEMPS = 835.0 DEGC
     TCUENA = ON
       GATE = ON
        NH3 = 95.0 SCCM
      PRCPR = 300. MTOR
  If    NH3 out-of-tolerance then
              goto ABRT
  If  PRCPR out-of-tolerance then
              goto ABRT
  If  VNTLK = ON then goto ABRT
  If  CABOT = ON then goto ABRT
  If  PRCPR > 1800. MTOR then goto
              ABRT
  If  GNTLK = ON then goto ABRT
  If TUBEOT = ON then goto ABRT
  If  SCROT = ON then goto ABRT
  If TEMPLC out-of-tolerance then
              goto ABRT
  If  TEMPC out-of-tolerance then
              goto ABRT
  If TEMPSC out-of-tolerance then
              goto ABRT

  If  DNTLK = ON then goto ABRT
  If  ANTLK = ON then goto ABRT
  If  BNTLK = ON then goto ABRT
STEP: 0200    COMMENT: POSTDEP
              PUMP 1TIME: 00.01.00
      TEMPL = 750.0 DEGC
     TEMPLC = 750.0 DEGC
      TEMPC = 750.0 DEGC
     TEMPSC = 750.0 DEGC
     TCUENA = ON
       GATE = ON
      TEMPS = 750.0 DEGC
  If  PRCPR > 1800. MTOR then goto
              ABRT
STEP: 0205    COMMENT: POSTDEP
              PURGE 1TIME:
              00.10.00
      TEMPL = 750.0 DEGC
     TEMPLC = 750.0 DEGC
      TEMPC = 750.0 DEGC
     TEMPSC = 750.0 DEGC
     TCUENA = ON
       GATE = ON
      TEMPS = 750.0 DEGC
        N2 = 500. SCCM
STEP: 0210    COMMENT: POSTDEP
              SONICTIME: 00.00.05
      TEMPL = 750.0 DEGC
     TEMPLC = 750.0 DE&C
      TEMPC = 750.0 DEGC
     TEMPSC = 750.0 DEGC
     TCUENA = ON
       GATE = ON
      TEMPS = 750.0 DEGC
      SONIC = ON
        N2 = 500. SCCM
STEP: 0215    COMMENT: POSTDEP
              HOLDTIME: 00.00.00
      TEMPL = 750.0 DEGC
     TEMPLC = 750.0 DEGC
      TEMPC = 750.0 DEGC
     TEMPSC = 750.0 DEGC
     TCUENA = ON
       GATE = ON
      TEMPS = 750.0 DEGC
        N2 = 500. SCCM
  If  EVENT = ON then goto 0220
STEP: 0220    COMMENT: BACKFILL 1
              TIME: 00.01.00
```

```
       TEMPL = 750.0 DEGC
      TEMPLC = 750.0 DEGC
       TEMPC = 750.0 DEGC
      TEMPSC = 750.0 DEGC
      TCUENA = ON
       TEMPS = 750.0 DEGC
          N2 = 500. SCCM
  If  EVENT = ON then goto CONT
STEP: 0225    COMMENT: BACKFILL 2
              TIME: 00.01.00
       TEMPL = 750.0 DEGC
      TEMPLC = 750.0 DEGC
       TEMPC = 750.0 DEGC
      TEMPSC = 750.0 DEGC
      TCUENA = ON
       TEMPS = 750.0 DEGC
          N2 = 1000. SCCM
STEP: 0230    COMMENT: BACKFILL 3
              TIME: 00.01.00
       TEMPL = 750.0 DEGC
      TEMPLC = 750.0 DEGC
       TEMPC = 750.0 DEGC
      TEMPSC = 750.0 DEGC
      TCUENA = ON
       TEMPS = 750.0 DEGC
          N2 = 2000. SCCM
STEP: 0235    COMMENT: BACKFILL 4
              TIME: 00.01.00
       TEMPL = 750.0 DEGC

      TEMPLC = 750.0 DEGC
       TEMPC = 750.0 DEGC
      TEMPSC = 750.0 DEGC
      TCUENA = ON
       TEMPS = 750.0 DEGC
          N2 = 3000. SCCM
STEP: 0240    COMMENT: BACKFILL 5
              TIME: 00.07.00
       TEMPL = 750.0 DEGC
      TEMPLC = 750.0 DEGC
       TEMPC = 750.0 DEGC
      TEMPSC = 750.0 DEGC
      TCUENA = ON
       TEMPS = 750.0 DEGC
          N2 = 5000. SCCM
STEP: 0245    COMMENT: POSTFILL
              SONICTIME: 00.00.05
       TEMPL = 750.0 DEGC
      TEMPLC = 750.0 DEGC
       TEMPC = 750.0 DEGC
      TEMPSC = 750.0 DEGC
      TCUENA = ON
       TEMPS = 750.0 DEGC
          N2 = 5000. SCCM
       SONIC = ON
STEP: 0250    COMMENT: POSTFILL
              HOLDTIME: 00.00.00
       TEMPL = 750.0 DEGC
      TEMPLC = 750.0 DEGC
       TEMPC = 750.0 DEGC
      TEMPSC = 750.0 DEGC
      TCUENA = ON
       TEMPS = 750.0 DEGC
          N2 = 5000. SCCM
  If  EVENT = ON then goto BTOT
STEP: BTOT    COMMENT: BOAT OUT
              TIME: 00.03.00
       TEMPL = 650.0 DEGC
      TEMPLC = 700.0 DEGC
       TEMPC = 700.0 DEGC
      TEMPSC = 700.0 DEGC
      TCUENA = ON
       TEMPS = 700.0 DEGC
  If  EVENT = ON then goto 0260
  If OUTLMT = ON then goto 0260
          N2 = 5000. SCCM
    BOATOUT = ON
    BOATSPD = 25.0 IPM
STEP: 0260    COMMENT: UNLOAD
              SONIC    TIME:
              00.00.05
       TEMPL = 650.0 DEGC
      TEMPLC = 700.0 DEGC
       TEMPC = 700.0 DEGC
      TEMPSC = 700.0 DEGC
      TCUENA = ON
       TEMPS = 700.0 DEGC
       SONIC = ON
          N2 = 5000. SCCM
  If  EVENT = ON then goto 0265
    BOATSPD = 25.0 IPM
STEP: 0265    COMMENT: UNLOAD
              TIME: 00.20.00
       TEMPL = 650.0 DEGC
      TEMPLC = 700.0 DEGC
       TEMPC = 700.0 DEGC
      TEMPSC = 700.0 DEGC
      TCUENA = ON
       TEMPS = 700.0 DEGC
  If  EVENT = ON then goto 0270
          N2 = 5000. SCCM
    BOATSPD = 25.0 IPM
STEP: 0270    COMMENT: BOAT IN FAST
              TIME: 00.03.00
       TEMPL = 650.0 DEGC
      TEMPLC = 700.0 DEGC
       TEMPC = 700.0 DEGC
      TEMPSC = 700.0 DEGC
      TCUENA = ON
       TEMPS = 700.0 DEGC
      BOATIN = ON
          N2 = 5000. SCCM
  If  INLMT = ON then goto 0275
    BOATSPD = 25.0 IPM
STEP: 0275    COMMENT: BOAT IN SLOW
              TIME: 00.02.00
       TEMPL = 750.0 DEGC
      TEMPLC = 750.0 DEGC
       TEMPC = 750.0 DEGC
      TEMPSC = 750.0 DEGC
      TCUENA = ON
       TEMPS = 750.0 DEGC
  If  DNTLK = ON then goto 0280
    BOATSPD = 5.0 IPM
```

```
         N2 = 5000. SCCM
      BOATIN = ON
STEP: 0280    COMMENT: ENDTIME:
              00.00.02
       TEMPL = 750.0 DEGC
      TEMPLC = 750.0 DEGC
       TEMPC = 750.0 DEGC
      TEMPSC = 750.0 DEGC
      TCUENA = ON
       TEMPS = 750.0 DEGC
         N2 = 5000. SCCM
SPECIAL HOLD STEP
STEP: SHLD    COMMENT: SPECIAL
              HOLD
       SONIC = ON
       TEMPL = 750.0 DEGC
      TEMPLC = 750.G DEGC
       TEMPC = 750.0 DEGC
      TEMPSC = 750.0 DEGC
       TEMPS = 750.0 DEGC
```

```
ABORT SEQUENCE
STEP: ABRT    COMMENT: PUMP 1TIME:
              00.05.00
       SONIC = ON
       TEMPL = N/C DEGC
        GATE = ON
      TEMPLC = N/C DEGC
       TEMPC = N/C DEGC
      TEMPSC = N/C DEGC
       TEMPS = N/C DEGC
STEP: A1      COMMENT: PURGE 1
              TIME: 00.02.00
         N2 = 200. SCCM
       TEMPL = N/C DEGC
      TEMPLC = N/C DEGC
       TEMPC = N/C DEGC
      TEMPSC = N/C DEGC
       TEMPS = N/C DEGC
        GATE = ON
  If   PRCPR > 1000. MTOR then goto
              SHLD
STEP: A2      COMMENT: PUMP 2TIME:
              00.05.00
        GATE = ON
       TEMPL = N/C DEGC
      TEMPLC = N/C DEGC
       TEMPC = N/C DEGC
      TEMPSC = N/C DEGC
       TEMPS = N/C DEGC
STEP: A3      COMMENT: PURGE 2
              TIME: 00.02.00
         N2 = 200. SCCM
       GATE = ON
       TEMPL = N/C DEGC
      TEMPLC = N/C DEGC
       TEMPC = N/C DEGC
      TEMPSC = N/C DEGC
       TEMPS = N/C DEGC
STEP: A4      COMMENT: PUMP 3TIME:
              00.05.00
       TEMPL = N/C DEGC
      TEMPLC = N/C DEGC
       TEMPC = N/C DEGC
      TEMPSC = N/C DEGC
       TEMPS = N/C DEGC
        GATE = ON
STEP: A5      COMMENT: PURGE 3
              TIME: 00.02.00
         N2 = 200. SCCM
       TEMPL = N/C DEGC
      TEMPLC = N/C DEGC
        GATE = ON
       TEMPC = N/C DEGC
      TEMPSC = N/C DEGC
       TEMPS = N/C DEGC
STEP: A10     COMMENT: HOLDTIME:
              00.00.00
         N2 = 200. SCCM
       TEMPL = N/C DEGC
      TEMPLC = N/C DEGC
       SONIC = ON
  If   PRCPR > 1000. MTOR then goto
              SHLD
       TEMPC = N/C DEGC
      TEMPSC = N/C DEGC
       TEMPS = N/C DEGC
        GATE = ON
  If   EVENT = ON then goto A11
  If      N2 < 100. SCCM then goto
              SHLD
STEP: All     COMMENT: BACKFILL 1
              TIME: 00.01.00
         N2 = 500. SCCM
       TEMPL = N/C DEGC
      TEMPLC = N/C DEGC
       TEMPC = N/C DEGC
      TEMPSC = N/C DEGC
       TEMPS = N/C DEGC
STEP: A12     COMMENT: BACKFILL 2
              TIME: 00.03.00
         N2 = 2000. SCCM
       TEMPL = N/C DEGC
      TEMPLC = N/C DEGC
       TEMPC = N/C DEGC
      TEMPSC = N/C DEGC
       TEMPS = N/C DEGC
STEP: A13     COMMENT: BACKFILL 3
              TIME: 00.07.00
         N2 = 5000. SCCM
       TEMPL = N/C DEGC
      TEMPLC = N/C DEGC
       TEMPC = N/C DEGC
      TEMPSC = N/C DEGC
       TEMPS = N/C DEGC

STEP: A14     COMMENT: BOAT OUT
              TIME: 00.10.00
     BOATSPD = 25.0 IPM
         N2 = 5000. SCCM
       TEMPL = 650.0 DEGC
      TEMPLC = 700.0 DEGC
       TEMPC = 700.0 DEGC
      TEMPSC = 700.0 DEGC
```

```
      TEMPS = 700.0 DEGC
    BOATOUT = ON
  If  EVENT = ON then goto A15
  If OUTLMT = ON then goto A15
STEP: A15     COMMENT: UNLOADTIME:
              00.15.00
         N2 = 5000. SCCM
  If  EVENT = ON then goto A16
      TEMPL = N/C DEGC
      SONIC = ON
     TEMPLC = N/C DEGC
      TEMPC = N/C DEGC
     TEMPSC = N/C DEGC
      TEMPS = N/C DEGC
STEP: A16     COMMENT: BOAT GOES IN
              TIME: 00.10.00
    BOATSPD = 10.0 IPM
         N2 = 5000. SCCM
      TEMPL = 650.0 DEGC
     TEMPLC = 750.0 DEGC
  If  DNTLK = ON then goto A17
      TEMPC = 750.0 DEGC
     TEMPSC = 750.0 DEGC
      TEMPS = 750.0 DEGC
     BOATIN = ON
STEP: A17     COMMENT: END ABRT
              TIME: 00.00.05
    BOATSPD = 7.5 IPM
      TEMPL = 750.0 DEGC
     TEMPLC = 750.0 DEGC
      TEMPC = 750.0 DEGC
     TEMPSC = 750.0 DEGC
      TEMPS = 750.0 DEGC
*** END OF FILE ***
```

Low Temperature Oxide (LTO) or Phospho-Silicate Glass (PSG)

```
LTO3LAYR.020
IDLE CONDITION
STEP: IDLE    COMMENT: IDLE STATE
      TEMPL = 450.0 DEGC
     TEMPLC = 450.0 DEGC
      TEMPC = 450.0 DEGC
     TEMPSC = 450.0 DEGC
      TEMPS = 450.0 DEGC
     TCUENA = ON
     N2BKFL = 1000. SCCM
```

```
PROCESS RUN SEQUENCE
STEP: STRT    COMMENT: SYSTM CHECK
              TIME: 00.00.10
      TEMPL = 450.0 DEGC
     TEMPLC = 450.0 DEGC
      TEMPC = 450.0 DEGC
     TEMPSC = 450.0 DEGC
      TEMPS = 450.0 DEGC
     TCUENA = ON
     N2BKFL = 1000. SCCM
  If     O2 > 4. SCCM then goto
              ABRT
  If  N2VAC > 10. SCCM then goto
              ABRT
  If   SIH4 > 2. SCCM then goto
              ABRT
  If  SCROT = ON then goto ABRT
  If    PH3 > .4 SCCM then goto
              ABRT
  If  TEMPL > 600.0 DEGC then goto
              ABRT
  If TEMPLC > 600.0 DEGC then goto
              ABRT
  If  TEMPC > 600.0 DEGC then goto
              ABRT
  If TEMPSC > 600.0 DEGC then goto
              ABRT
  If  TEMPS > 600.0 DEGC then goto
              ABRT
  If  CABOT = ON then goto ABRT
  If TUBEOT = ON then goto ABRT
STEP: 0005    COMMENT: UNLOAD
              TIME: 00.03.00
      TEMPL = 450.DEGC
     TEMPLC = 450.0 DEGC
      TEMPC = 450.0 DEGC
     TEMPSC = 450.0 DEGC
      TEMPS = 450.0 DEGC
     TCUENA = ON
     N2BKFL = 1000. SCCM
    BOATSPD = 25.0 IPM
    BOATOUT = ON
  If OUTLMT = ON then goto 0010
  If  CABOT = ON then goto ABRT
  If  EVENT = ON then goto 0010
STEP: 0010    COMMENT: LOAD SONIC
              TIME: 00.00.03
      TEMPL = 450.DEGC
     TEMPLC = 450.0 DEGC
      TEMPC = 450.0 DEGC
     TEMPSC = 450.0 DEGC
      TEMPS = 450.0 DEGC
     TCUENA = ON
     N2BKFL = 1000. SCCM
      SONIC = ON
  If  CABOT = ON then goto ABRT
STEP: 0015    COMMENT: LOAD ON
              EVENT TIME: 00.20.00
      TEMPL = 420.DEGC
     TEMPLC = 420.0 DEGC
      TEMPC = 420.0 DEGC
     TEMPSC = 420.0 DEGC
      TEMPS = 420.0 DEGC
```

```
     TCUENA = ON
     N2BKFL = 1000. SCCM
      SONIC = ON
  If  EVENT = ON then goto BTIN
  If  CABOT = ON then goto ABRT
STEP: BTIN    COMMENT: BOAT IN FAST
              TIME: 00.03.00
     N2BKFL = 1000. SCCM
     TCUENA = ON
      TEMPS = 450.DEGC
     TEMPSC = 450.0 DEGC
      TEMPC = 450.0 DEGC
     TEMPLC = 450.0 DEGC
      TEMPL = 450.0 DEGC
     BOATIN = ON
    BOATSPD = 25.0 IPM
  If  INLMT = ON then goto 0025
  If  CABOT = ON then goto ABRT
STEP: 0025    COMMENT: BOAT IN SLOW
              TIME: 00.02.00
     N2BKFL = 1000. SCCM
     TCUENA = ON
      TEMPS = 450.DEGC
     TEMPSC = 450.0 DEGC
      TEMPC = 450.0 DEGC
     TEMPLC = 450.0 DEGC
      TEMPL = 450.0 DEGC
     BOATIN = ON
    BOATSPD = 5.0 IPM
  If  INLMT = OFF then goto BTIN
  If  DNTLK = OFF then goto 0030
STEP: 0030    COMMENT: PUMP DOWN
              TIME: 00.02.00
     TCUENA = ON
      TEMPS = 450.0 DEGC
     TEMPSC = 450.0 DEGC
      TEMPC = 450.0 DEGC
       GATE = ON
     TEMPLC = 450.0 DEGC
      TEMPL = 450.0 DEGC
  If  DNTLK = ON then goto ABRT
STEP: 0035    COMMENT:N2 PURGE
              TIME: 00.02.00
     TCUENA = ON
      TEMPS = 450.0 DEGC
     TEMPSC = 450.0 DEGC
      TEMPC = 450.0 DEGC
       GATE = ON
     TEMPLC = 450.0 DEGC
      TEMPL = 450.0 DEGC
     N2BKFL = 150. SCCM
  If  EVENT = ON then goto 0040
STEP: 0040    COMMENT: HARD PUMP
              TIME: 00.02.00
     TCUENA = ON
      TEMPS = 450.0 DEGC
     TEMPSC = 450.0 DEGC
      TEMPC = 450.0 DEGC
       GATE = ON
     TEMPLC = 450.0 DEGC
      TEMPL = 450.0 DEGC
  If  EVENT = ON then goto 0045
STEP: 0045    COMMENT: LEAK CHECK
              TIME: 00.01.00
     TCUENA = ON
      TEMPS = 450.0 DEGC
     TEMPSC = 450.0 DEGC
      TEMPC = 450.0 DEGC
  If  EVENT = ON then goto 0050
     TEMPLC = 450.0 DEGC
      TEMPL = 450.0 DEGC
  If  PRCPR > 60. MTOR then goto
              ABRT
STEP: 0050    COMMENT: PUMP ON
              TIME: 00.02.00
     TCUENA = ON
      TEMPS = 450.DEGC
     TEMPSC = 450.0 DEGC
      TEMPC = 450.0 DEGC
     TEMPLC = 450.0 DEGC
      TEMPL = 450.0 DEGC
       GATE = ON
  If  EVENT = ON then goto 0055
STEP: 0055    COMMENT: PURGE N2 ON
              TIME: 00.01.00
     TCUENA = ON
      TEMPS = 450.DEGC
     TEMPSC = 450.0 DEGC
      TEMPC = 450.0 DEGC
     TEMPLC = 450.0 DEGC
      TEMPL = 450.0 DEGC
       GATE = ON
      PRCPR = 300. MTOR
     N2BKFL = 180. SCCM
STEP: 0060    COMMENT: TEMP STABI-
              LIZETIME: 00.02.00
     TCUENA = ON
      TEMPS = 450.DEGC
     TEMPSC = 450.0 DEGC
      TEMPC = 450.0 DEGC
     TEMPLC = 450.0 DEGC
      TEMPL = 450.0 DEGC
       GATE = ON
      PRCPR = 300. MTOR
  If  EVENT = ON then goto 0070
  If  DNTLK = ON then goto ABRT
  If  BNTLK = ON then goto ABRT
  If  GNTLK = ON then goto ABRT
  If  CABOT = ON then goto ABRT
  If  SCROT = ON then goto ABRT
  If TUBEOT = ON then goto ABRT
STEP: 0065    COMMENT: TEMP CHECK
              TIME: 00.02.00
     TCUENA = ON
      TEMPS = 450.0 DEGC
     TEMPSC = 450.0 DEGC
      TEMPC = 450.0 DEGC
     TEMPLC = 450.0 DEGC
      TEMPL = 450.0 DEGC
       GATE = ON
      PRCPR = 300. MTOR
  If  DNTLK = ON then goto ABRT
  If  BNTLK = ON then goto ABRT
```

```
  If  TEMPS < 448.0 DEGC then goto
              0060
  If  GNTLK = ON then goto ABRT
  If  TEMPL > 452.0 DEGC then goto
              0060
  If  TEMPL < 448.0 DEGC then goto
              0060
  If TEMPLC > 451.0 DEGC then goto
              0060
  If TEMPLC < 449.0 DEGC then goto
              0060
  If  TEMPC > 451.0 DEGC then goto
              0060
  If  TEMPC < 449.0 DEGC then goto
              0060
  If TEMPSC > 451.0 DEGC then goto
              0060
  If TEMPSC < 449.0 DEGC then goto
              0060
  If  TEMPS > 452.0 DEGC then goto
              0060
STEP: 0070  COMMENT: HARD PUMP
              TIME: 00.01.00
     TCUENA = ON
      TEMPS = 450.0 DEGC
     TEMPSC = 450.0 DEGC
      TEMPC = 450.0 DEGC
     TEMPLC = 450.0 DEGC
      TEMPL = 450.0 DEGC
       GATE = ON
  If  DNTLK = ON then goto ABRT
  If  BNTLK = ON then goto ABRT
  If  GNTLK = ON then goto ABRT
  If  CABOT = ON then goto ABRT
STEP: 0080    COMMENT: FIRST LAYER
              TIME: variable/
              00.05.00
     TCUENA = ON
      TEMPS = 450.0 DEGC
     TEMPSC = 450.0 DEGC
      TEMPC = 450.0 DEGC
     TEMPLC = 450.0 DEGC
      TEMPL = 450.0 DEGC
       GATE = ON
         02 = 90. SCCM
       SIH4 = 60. SCCM
        PH3 = variab/ 5.0 SCCM
      PRCPR = 300. MTOR
  If  EVENT = ON then goto 0085
  If  DNTLK = ON then goto ABRT
  If  BNTLK = ON then goto ABRT
  If  GNTLK = ON then goto ABRT
  If  CABOT = ON then goto ABRT
STEP: 0081    COMMENT: SECOND
              LAYERTIME: variable/
              00.01.00
     TCUENA = ON
      TEMPS = 450.0 DEGC
     TEMPSC = 450.0 DEGC
      TEMPC = 450.0 DEGC
     TEMPLC = 450.0 DEGC
      TEMPL = 450.0 DEGC
       GATE = ON
         02 = 90. SCCM
       SIH4 = 60. SCCM
        PH3 = variab/ 5.0 SCCM
      PRCPR = 300. MTOR
  If  EVENT = ON then goto 0085
STEP: 0082    COMMENT: THIRD LAYER
              TIME: variable/
              00.01.00
     TCUENA = ON
      TEMPS = 450.0 DEGC
     TEMPSC = 450.0 DEGC
      TEMPC = 450.0 DEGC
     TEMPLC = 450.0 DEGC
      TEMPL = 450.0 DEGC
       GATE = ON
         02 = 90. SCCM
       SIH4 = 60. SCCM
        PH3 = variab/ 5.0 SCCM
      PRCPR = 300. MTOR
  If  EVENT = ON then goto 0085
STEP: 0085    COMMENT: GASES OFF-
              PUMPTIME: 00.02.00
     TCUENA = ON
      TEMPS = 450.0 DEGC
     TEMPSC = 450.0 DEGC
      TEMPC = 450.0 DEGC
     TEMPLC = 450.0 DEGC
      TEMPL = 450.0 DEGC
       GATE = ON
STEP: 0090    COMMENT: N2 ON -
              SONICTIME: 00.01.00
     TCUENA = ON
      TEMPS = 450.0 DEGC
     TEMPSC = 450.0 DEGC
      TEMPC = 450.0 DEGC
     TEMPLC = 450.0 DEGC
      TEMPL = 450.0 DEGC
       GATE = ON
     N2BKFL = 150. SCCM
      SONIC = ON
  If  EVENT = ON then goto 0095
STEP: 0095    COMMENT: FLUSH AND
              HOLDTIME: 00.00.00
     TCUENA = ON
      TEMPS = 450.0 DEGC
     TEMPSC = 450.0 DEGC
      TEMPC = 450.0 DEGC
     TEMPLC = 450.0 DEGC
      TEMPL = 450.0 DEGC
       GATE = ON
  If  EVENT = ON then goto 0100
     N2BKFL = 150. SCCM
STEP: 0100    COMMENT: NORMAL
              BACKFILL
              TIME: 00.05.00
     TCUENA = ON
      TEMPS = 450.0 DEGC
     TEMPSC = 450.0 DEGC
      TEMPC = 450.0 DEGC
     TEMPLC = 450.0 DEGC
      TEMPL = 450.0 DEGC
```

```
     N2BKFL = 5000. SCCM
STEP: 0105    COMMENT: SONIC
              TIME: 00.00.05
     TCUENA = ON
      TEMPS = 450.0 DEGC
     TEMPSC = 450.0 DEGC
      TEMPC = 450.0 DEGC
     TEMPLC = 450.0 DEGC
      TEMPL = 450.0 DEGC
     N2BKFL = 5000. SCCM
      SONIC = ON
STEP: BTOT    COMMENT: UNLOAD
              TIME: 00.04.00
     TCUENA = ON
      TEMPS = 450.0 DEGC
     TEMPSC = 450.0 DEGC
      TEMPC = 450.0 DEGC
     TEMPLC = 450.0 DEGC
      TEMPL = 450.0 DEGC
     N2BKFL = 1000. SCCM
    BOATOUT = ON
    BOATSPD = 25.0 IPM
  If 0UTLMT = ON then goto 0115
STEP: 0115  COMMENT: END     TIME:
              00.00.02
     TCUENA = ON
      TEMPS = 450.0 DEGC
     TEMPSC = 450.0 DEGC
      TEMPC = 450.0 DEGC
     TEMPLC = 450.0 DEGC
      TEMPL = 450.0 DEGC
     N2BKFL = 1000. SCCM
SPECIAL HOLD STEP
STEP: SHLD    COMMENT: SPECIAL
              HOLD
      TEMPL = 450.0 DEGC
     TEMPLC = 450.0 DEGC
      TEMPC = 450.0 DEGC
     TEMPSC = 450.0 DEGC
      TEMPS = 450.0 DEGC
     TCUENA = ON
     N2BKFL = 1000. SCCM
      SONIC = ON
```

```
ABORT SEQUENCE
STEP: ABRT    COMMENT: ABORT
              TIME: 00.00.15
      TEMPL = 450.O DEGC
     TEMPLC = 450.0 DEGC
      TEMPC = 450.0 DEGC
     TEMPSC = 450.0 DEGC
      TEMPS = 450.0 DEGC
     TCUENA = ON
      SONIC = ON
     N2BKFL = 200. SCCM
```

B.2 Plasma Etch

Oxide

These recipes, listed in Table B.1 and Table B.2, run on a LAM Research Corporation AutoEtch.

Table B.1 Standard oxide etch recipe

SIO2ET.RCP		Step					
Parameter	Unit	1	2	3	4	5	6
Pressure	Torr	2.8	2.8	3.0	3.0	0	
RF Top	W	0	850	0	700	0	
Gap	cm	0.38	0.38	0.40	0.40	1.35	
C2F6	sccm	0	0	0	0	0	
O2	sccm	0	0	0	0	0	
He	sccm	120	120	110	110	0	
CHF3	sccm	30	30	35	35	0	
CF4	sccm	90	90	30	30	0	
Time or End Condition	min:s	:30 or Stable	1:45 or End-point	:20 or Stable	:20	:10	End of Recipe

In this thesis all of the oxide etches are timed. If an etch requires more than 1:45, use the long recipe shown in Table B.2 and adjust the total etch time by moving the end of recipe command and shortening the last etch step. Do not increase the etch time in any step.

Table B.2 Long oxide etch recipe

LONGSIO2.RCP		Step								
Parameter	Unit	1	2	3	4	5	6	7	8	9
Pressure	Torr	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	
RF Top	W	0	850	0	850	0	850	0	850	
Gap	cm	0.38	0.38	0.38	0.38	0.38	0.38	0.38	0.38	
C2F6	sccm	0	0	0	0	0	0	0	0	
O2	sccm	0	0	0	0	0	0	0	0	
He	sccm	120	120	120	120	120	120	120	120	
CHF3	sccm	30	30	30	30	30	30	30	30	
CF4	sccm	90	90	90	90	90	90	90	90	
Time or End Condition	min:s	:30 or Stable	1:30 or End-point	1:00	1:30 or End-point	1:00	1:30 or End-point	1:00	1:30 or End-point	End of Rec-ipe

Polysilicon

The recipe shown in Table B.3is run on a Lam Research Corporation “Rainbow” etcher. It includes a short pre-etch to remove native oxide, and a highly selective overetch.

Table B.3 Polysilicon etch recipe

Recipe: 5003		Step							
Paramet	Unit	1	2	3	4	5	6	7	8
Pressure	mTorr	0.00	13.00	13.00	15.00	15.00	80	80	
RF Top	W	0	0	200	0	300	0	200	
RF Bottom	W	0	0	40	0	150	0	150	
Gap	cm	5.80	5.80	5.80	5.80	5.80	5.80	5.80	
CL2	sccm	0	0	0	50.0	50.0	0	0	
HBr	sccm	0	0	0	150.0	150.0	100	100	
CHF3	sccm	0	0	0	0	0	0	0	
O2	sccm	0	0	0	0	0	1.0	1.0	
He/Ar	sccm	0	0	0	0	0	100	100	
SF6	sccm	0	0	0	0	0	0	0	
O2	sccm	0	0	0	0	0	0	0	
CF4	sccm	0	100	100	0	0	0	0	
He clamp	t	0	4.0	4.0	4.0	4.0	4.0	4.0	
Complete		stab	stab	time	stab	endpt	stab	oetch	end
Time	sec	20	30	10	30	30	30	20%	
Channel						A			
Delay	sec					15			
Norm	sec					10			
Norm Value						5000			
Trigger	%					75			
Slope	cs/s								

Aluminum

The recipes shown in Table B.4 and Table B.5 use a Lam Aluminum RIE Etcher model 690. In addition to the regular process or REACTOR chamber, the 960 has a plasma load lock where a post treatment of the wafers is done. A built-in endpoint detector is available for determining etch time.

Table B.4 Standard aluminum etch reactor recipe

		Step				
Parameter	Unit	1	2	3	4	5
Pressure	mTorr	250.0	250.0	250.0	000.0	
RF Lower	watts	000.0	250.0	250.0	000.0	
BCl3	sccm	050.0	050.0	050.0	000.0	
N2	sccm	050.0	50.0	50.0	100.0	
Cl2	sccm	30.0	30.0	20.0	000.0	
CHCl3	sccm	020.0	020.0	020.0	000.0	
SF6	sccm	000.0	000.0	000.0	000.0	
Complete		Stability or Time	Time & Endpoint	Overetch	Time	Recipe
Max	min:s	00:20	03:00	50%	00:10	

Table B.5 Standard aluminum etch airlock recipe

	1	1	Step
Parameter	Unit	1	2
Pressure	torr	1.0	0.0
RF Top	watts	400.0	000.0
Gas1	sccm	000.0	000.0
Gas2 (CF4)	sccm	090.0	000.0
Gas3 (O2)	sccm	010.0	000.0
Completion	mode	Time	Recipe
Max	min:sec	01:00	00:00

Photoresist Descum

The descum process listed in Table B.6 is used to remove undeveloped photoresist that may be lurking in small holes and around edges before hard-baking.

Table B.6 Descum recipe

Parameter	Units	Step 1
Pressure	mTorr	270-280
Power	watts	50
O2	sccm	51.1
Time	min.	1.0

Photoresist Ashing

To remove photoresist, particularly if it has been hard-baked, after a plasma etch, use the ashing recipe given in Table B.7.

Table B.7 Photoresist ashing recipe

Parameter	Units	Step 1
Pressure	mTorr	270-280
Power	watts	300
O2	sccm	51.1
Time	min.	7

B.3 CMP

The cemical-mechanical polishing recipe listed in Table B.8 is the best I tried for uniformity across the wafer. It appears to give better results if backside compressive films are removed so that the wafers are flat or bowed up in the center.

Table B.8 CMP recipe

		Step				
Paramter	Unit	1	2	3	4	5
Time	sec.	15	5	5	30[a]	15
Downforce	psi	0	2	5	8	2
Table Speed	rpm	75	75	75	75	75
Chuck Speed	rpm	6	6	6	6	6
Back Pressure	psi	-2	-2	-2	1	-2
Temperature	°C	30	30	30	30	30
Slurry	cc/min	150	50	50	50	0
Rinse	off	off	off	off	off	on

a. Polishing time should be a multiple of 5 seconds to give the wafer an integer number of half-turns. For best results, polish for 1/2 of the desired time and then reposition the chuck 1/2 revolution from original starting position and then polish the remaining time.

B.4 Self-Assembled Monolayer (SAM) coating

```
                Self-Assembled Monolayer Coating Process
                            Version 2.2
                            (09-17-97)


*** Process normally executed immediately after aqueos release step. ***
*** SAM coating can be used in conjunction with critical point drying. *
*** OTS and PFDTS SAM coating documented.  Refer to steps 5 & 6.     ***
```

1.0 Structural Release

a) Wet etch: concentrated (49%) HF
b) DI dilution rinse

notes:
i) This MUST be done in total darkness if CMOS circuitry attached to exposed polysilicon. Avoids photochemical etching of circuit bondpads.
ii) Include bare Si chiplet for contact angle measurement.
iii) Alternative release fluids may be used. Depends upon structural/sacrificial layers (i.e. KOH would be used w/ Si3N4 structural and Al sacrificial layers).

2.0 Polysilicon Reoxidation

a) DI rinse: 10 min.
(a continuation of step 1.0b) above)
b) H2O2 soak (30% assay): 10 min.
(careful, this step may attack exposed aluminum)
c) DI rinse: 2 min.

note: post-release sulfuric peroxide could substitute H2O2

3.0 Aqueous Dehydration 1

a) IPA (or methanol): dilution/rinse
b) Transfer sample to bath of IPA. Soak for 5min.
c) Transfer sample to 2nd bath of IPA. Soak for 5min.

notes:
i) Dilution/rinse: Pour IPA into previous DI rinse while aspirating until DI is completely displaced. Rinse for 5 min.
ii) Never expose structures to air.
iii) IPA or methanol fully miscible in iso-octane.

4.0 Aqueous Dehydration 2 (iso-octane soak)

a) Transfer sample to fresh iso-octane. Soak for 5 min.
b) Transfer sample to 2nd fresh bath of iso-octane. Soak 5 min.

notes:
i) iso-octane = 2,2,4 trimethylpentane
ii) Never expose strucutures to air.
iii) iso-octane fully miscible in SAM solution.

5.0 Self-Assembled Monolayer Coating

option 1: OTS

a) OTS SAM solution mix
   i) SAM solution - 4:1 hexadecane:chloroform + 1 drop OTS per 50 ml solvent (full wafer needs 80ml hexadecane and 20ml chloroform)
   ii) hexadecane = CH3(CH2)14CH3
   chloroform = CHCl3
   OTS = octadecyltrichlorosilane CH3(CH2)17SiCl3
   iii) 1 drop = 5 ul ==> dilution of OTS to achieve 1mM
   iv) do not oversaturate solution with OTS, better to have a weaker solution and longer soak.
   v) Mix solution in drybox. Remove and let stand in air for 5 min prior to using.
   vi) Use Teflon or glass petri dish. Clean and dehydrate dishes prior to use. Do not use polystyrene.

b) Transfer sample to OTS SAM. Soak for 15 min.

option 2: PFDTS

a) Transfer iso-octane soaking dish into drybox. Also transfer two empty dishes at this time to be used for iso-octane soaking.

b) PFDTS SAM solution mix
   i) SAM solution - iso-octane + 1-3 drops PFDTS per 50 ml solvent (full wafer needs 100 ml iso-octane)
   ii) iso-octane = 2,2,4 trimethylpentane
   PFDTS=1H,1H,2H,2H-perfluorodecyltrichlorosilane CF3(CF2)7(CH2)2SiCl3
   iii) 1 drop = <5 ul ==> dilution of PFDTS to achieve 1mM (high surface tension results in very small drops)
   iv) Exact concentration of PFDTS not critical.
   v) Mix and use solution in drybox.
   vi) OK to use polystyrene petri dish.
   vii) Do not expose solution to air at any time.

c) Transfer sample to PFDTS SAM. Soak for 5-10 min. (PFDTS more reactive than OTS ==> less coating time required)

6.0 Reversed Organinc Rinsing
a) Dilute SAM solution with iso-octane to 1:1 ratio. Soak 5 min. <== OTS process only. Skip if using PFDTS.
b) Transfer sample to fresh iso-octane bath. Soak 5 min.
c) Transfer sample to fresh IPA bath. Soak 5 min.
d) Transfer sample to 2nd fresh IPA bath. Soak 5 min.

notes:

i) In the case of PFDTS SAM skip step a) but repeat step b) -both to be done inside the drybox. Fresh iso-octane not required as PFDTS is already diluted in pure iso-octane - resuse solutions in drybox. Final transfer to IPA may be done outside drybox. Extreme hydrophobicity can cause dewetting during any transfer. Not a problem since PFDTS-->iso-octane transfers are done in drybox.

ii) Reverse rinsing back to DI water required because it is necessary for the final dewet to be from a high surface tension liquid. This will result in SAM-coated surfaces with contact angles greater than 90 deg.

iii) Do not aspirate iso-octane and OTS or PFDTS solutions. Use the organic disposal bottles provided at sink.

7.0 Final rinse ---> note options

option 1: DI rinse followed by a direct pull.

notes:

i) Surface should be hydrophobic enough (i.e. contact angle > 110 deg.) to prevent water from remaining.

ii) This "direct pull" method is topography sensitive.

iii) Both OTS and PFDTS require DI rinse as final step.

option 2: Direct transfer of IPA (or methanol) soaked wafer to methanol-charged critical point drying station. CO_2 critical point drying as per CPD operating procedures.

---

general notes:

i) All glassware used should be cleaned/rinsed/baked prior to use with solvent chemistries.

ii) May be best to dedicate PFDTS glassware and/or plasticware as cross-contamination may occur.

iii) All organic chemicals should be of anhydrous grade.

iv) OTS and/or PFDTS should be purchased in small quantities and stored in purged drybox. Micropipette dispense is best.

Developed by: M. Houston / T. Srinivasan
Documented by: J. Bustillo / rev. 1.0 / 06/19/96
/ rev. 2.0 / 05/19/97

---

revision changes

revision	comments
1.0	original SAM process flow documented as per M.H.

```
1.1    sec. 4.1: specify iso-octane soak times
2.0    sec. 3.0: 5 min rinse followed by 5 min soak
       sec. 4.0: direct transfer from IPA to iso-octane.
             two 5 min soaks.
       sec. 5.0: specify volume of "drop"
             add notes describing OTS exposure to air prior to use
             add PFDTS procedures as option 2
       sec. 6.0: specify individual soak times for reversed rinses
             add PFDTS notes
2.1    sec. 2.0: H2O2 soak = 5 min.
       sec. 3.0: add step c) ==> 2nd 5 min. IPA soak.
       sec. 6.0: add step d) ==> 2nd 5 min. IPA soak.
                 add verbage about high surface tension DI dewet
2.2    sec. 5.0: Do not use polystyrene petri dish for OTS SAM.
end
```

Appendix C. MathCad Sheets

This sheet defines the Rotated Box function used to rotate rectangles for the pattern generator. The input dimensions are in microns for ease of design and the output units are for use directly in KIC text files assuming that lambda = 0.1 micron. Simply cut and paste the eight number output onto a line beginning with a P for polygon and end it with a semicolon.

Rotation of Boxes

Inputs:
Desired box size x,y, center x, center y, angle of rotation

$$l(x,y) := \sqrt{\frac{x^2 + y^2}{4}}$$

$$Rotbox(x,y,cx,cy,\theta) := floor\left[\left[\begin{bmatrix} \cos(angle(x,y)+\theta) \\ \sin(angle(x,y)+\theta) \\ \cos(angle(-x,y)+\theta) \\ \sin(angle(-x,y)+\theta) \\ \cos(angle(-x,-y)+\theta) \\ \sin(angle(-x,-y)+\theta) \\ \cos(angle(x,-y)+\theta) \\ \sin(angle(x,-y)+\theta) \end{bmatrix}^T \cdot l(x,y) + \begin{bmatrix} cx \\ cy \\ cx \\ cy \\ cx \\ cy \\ cx \\ cy \end{bmatrix}^T\right] \cdot 1000 + .5\right]$$

$$round(x,n) := floor\left(x \cdot 10^n + .5\right) \cdot 10^{-n}$$

$q := angle(3,2)$ $q = 33.69 \cdot deg$ $s := angle(4,1)$ $s = 14.036 \cdot deg$

$$l(24,16) \cdot 2 = 28.844$$

Note that the GCA 3600 pattern generator can rotate boxes in tenths of degrees.

$Rotbox(4,8,-1,3,90 \cdot deg) = (-5000 \quad 5000 \quad -5000 \quad 1000 \quad 3000 \quad 1000 \quad 3000 \quad 5000)$

$Rotbox(6,6,-20,0,-14 \cdot deg) = (-16363 \quad 2185 \quad -22185 \quad 3637 \quad -23637 \quad -2185 \quad -17815 \quad -3637)$

$Rotbox(2,60,-20,0,-14 \cdot deg) = (-11772 \quad 28867 \quad -13713 \quad 29351 \quad -28228 \quad -28867 \quad -26287 \quad -29$

$$Rotbox\left(60,32,\frac{65+17}{\sqrt{2}},\frac{65-17}{\sqrt{2}},45 \cdot deg\right) = (67882 \quad 66468 \quad 25456 \quad 24042 \quad 48083 \quad 1414 \quad 90510 \quad 4$$

When an array of rotated boxes was needed for an arc or a structure like the strain guage, I used this sheet to generate a file.

Multiple rotated box structures located along an arc:

Enter number of boxes:

$N := 72$

Enter the center co-ordinates of the arc and radius to center of boxes (x and y and r in microns

$x := 0 \qquad y := 0 \qquad r := 450$

Enter the stepping angle along the arc between box centers
(remember the GCA handles tenths of a degree):

$\Theta_{step} := 5 \cdot deg \qquad \Theta_{step} = 5 \circ deg$

Enter the starting angle for the arc assuming counter clockwise rotation(3 o'clock is zero angle

$\Theta_{start} := 0 \cdot \Theta_{step}$

Enter the size of each box (x and y) in microns assuming its orientation is at zero angle:
(if this structure is to be connected - a circle or arc - make ysize equal to ycont.)

$x_{size} := 10 \qquad y_{cont} := \left(2 \cdot r + x_{size}\right) \cdot \tan\left(\frac{\Theta_{step}}{2}\right) \qquad y_{size} := y_{cont}$

$i := 0 .. N - 1$

$\Theta_i := \Theta_{start} + i \cdot \Theta_{step} \qquad c := 0 .. 7$

$$A_{i,c} := \left(Rotbox\left(x_{size}, y_{size}, x + r \cdot \cos\left(\Theta_i\right), y + r \cdot \sin\left(\Theta_i\right), round\left(\frac{\Theta_i}{deg}, 1\right) \cdot deg \right)^T \right)_c$$

The following line writes out the kic polygon co-ordinates for the boxes to the file arc.prn

$WRITEPRN("arc.prn") := A$

Calculation of torque on the mirror generated by application of voltage on the data lines.

ASSUME: That the area involved is only that above the data electrodes. No edge effects are considered.

Red and Blue Mirror Pixel geometry:

$L_y := 58\ \mu m$ $L_x := 18\ \mu m$ $L_{dash} := \frac{1}{2}\cdot\sqrt{L_x^2 + L_y^2}$ $\theta_{pad} := \operatorname{atan}\left(\frac{L_x}{L_y}\right)$

$\theta_{spring} := 14\ deg$ $R_{max} := L_{dash}\cdot\sin\left(\theta_{spring} + \theta_{pad}\right)$ $R_{max} = 15.748\cdot\mu m$

$\theta_{tilt} := 10\cdot deg$ $D := 2\cdot R_{max}\cdot\tan\left(\frac{\theta_{tilt}}{2}\right)$ $D = 2.756\cdot\mu m$

$L_{py} := 24\ \mu m$ $L_{px} := 9\ \mu m$ $L_{diag} := \sqrt{L_{py}^2 + L_{px}^2}$ $Pad\theta := \operatorname{atan}\left(\frac{L_{px}}{L_{py}}\right)$

$R_{pad} := L_{diag}\cdot\sin\left(\theta_{spring} + Pad\theta\right)$ $R_{pad} = 14.539\cdot\mu m$

$W_{base} := \frac{L_{py}}{\cos\left(\theta_{spring}\right)} + \frac{L_{px}}{\sin\left(\theta_{spring}\right)}$ $W_{base} = 61.9\cdot\mu m$

$gap := \frac{8\ \mu m}{\cos\left(\theta_{spring}\right)}$ $gap = 8.245\cdot\mu m$ $R_{min} := 3\ \mu m$

$L := R_{pad}$ $range := 0\cdot\mu m, 0.5\cdot\mu m .. L$

$W_{pad}(r) := \text{if}\left[|r| < R_{min}, 0\cdot\mu m, \left[\text{if}\left[(|r| < 10\ \mu m), \left[\left(\frac{L - |r|}{L}\right)\cdot W_{base} - gap\right], \frac{L - |r|}{L}\cdot W_{base}\right]\right]\right]$

Distance between plates $d(r,\theta) := D - 2\cdot r\cdot\tan\left(\frac{\theta}{2}\right)$ $D = 2.756\cdot 10^{-6}\ m$

Field strength $E(r,\theta,v) := \frac{v}{d(r,\theta)}$ $d\left(R_{pad}, \theta_{tilt}\right) = 0.212\cdot\mu m$

Capacitance per length $C(r,\theta) := \varepsilon_0\cdot\frac{W_{pad}(r)}{d(r,\theta)}$

Charge per length $Q(r,\theta,v) := C(r,\theta)\cdot v$

Force per length $F(r,\theta,v) := E(r,\theta,v)\cdot Q(r,\theta,v)$

Torque per length $T(r,\theta,v) := F(r,\theta,v)\cdot r$

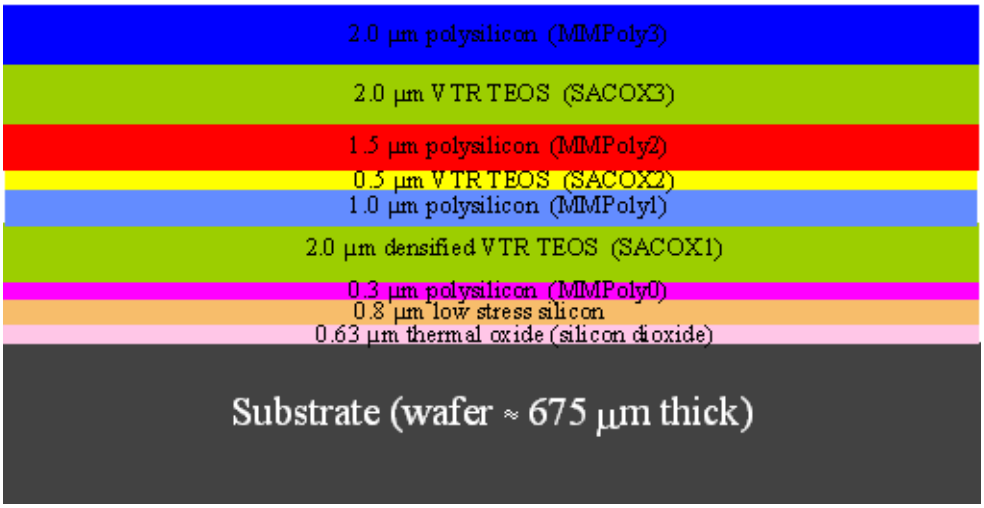
Appendix D. Sandia Process

The following document was provided to BSAC students to document the process made available to us at Sandia National Laboratories. (Used with permission)

D.1 Process Tutorial

The cross section of an unpatterned wafer shown below in Figure D.1 illustrates the various material layers comprising the SUMMiT fabrication process. Note that above the low-stress silicon nitride layer alternating layers of polysilicon and sacrificial oxide occur. The film thicknesses are specified as part of the baseline process, and are not parameters that can be changed.

Figure D.1 Unpatterned cross section of SUMMiT wafer



SUMMiT designs are laid out using AutoCAD R14. Each layer in the SUMMiT process is patterned and etched according to a mask. The combination of masks defining each layer is called a mask set. The mask set has an associated AutoCAD drawing which contains design layouts of all the layers. Layer names, mask level descriptions, film

descriptions, and layer purpose are defined in the following table.

Table D.1 Fabrication layers — top-down

Layer	Mask level(s)	Film description	Purpose
MMPoly3	MMPoly3 xor MMPoly3_Cut	2.25 µm doped, planar polySi	Mechanical polySi #3
SacOx3	SacOx3_Cut, Dimple3	1.5 - 2 µm planarized TEOS	Sacrificial oxide, anchor
MMPoly2	MMPoly2 xor MMPoly2_Cut	1.5 µm doped polySi	Mechanical polySi #2
SacOx2	SacOx2 xor SacOx2_Cut	0.5 µm TEOS	Sacrificial oxide, hub clearance
MMPoly1	MMPoly1_Cut xor MMPoly 1, Pin_Joint_Cut	1.0 µm doped polySi	Mechanical polySi #1, hub for gears
SacOx1	SacOx1_Cut, Dimple1	2 µm TEOS	Sacrificial oxide, anchor
MMPoly0	MMPoly0	0.3 µm doped polySi	Ground plane
Nitride	Nitride_Cut	0.8 µm SiNx over 0.6 µm SiO2	Electrical isolation

Throughout the development of the AutoCAD layout, periodic use of the Design Rule Checker (DRC) is recommended. The DRC aids in detecting design errors that can result in fabrication problems. The DRC operates on GDSII file formats, thus, the AutoCAD file is first translated into a GDSII file before the DRC runs. The table that follows describes the various SUMMiT mask levels and the corresponding GDSII code designation (2 digit number), the Design Rule Checker code designation, the AutoCAD layer color, and the purpose of the mask level.

Table D.2 SUMMiT mask levels and colors

Mask Level	Code	Color	Purpose
21 Nitride_Cut [a]	NIC	Purple	Substrate contacts
22 MMPoly0	P0	Magenta	Ground plane
23 Dimple1_Cut	D1C	Dk Blue	Dimples in P1
24 SacOx1_Cut	X1C	Green	Anchor P1
25 MMPoly1_Cut	P1C	Black	Holes in P1, no flange
26 Pin_Joint_Cut	PJC	Yellow	Holes in P1 w/flange

Table D.2 SUMMiT mask levels and colors

Mask Level	Code	Color	Purpose
27 SacOx2	X2	Tan	Separate P1 & P2
28 MMPoly2	P2	Red	Define shapes in P2 and/or P1+P2
29 Dimple3_Cut	D3C	Yellow	Dimples in P3
30 SacOx3_Cut	X3C	Black	Anchor P3
31 MMPol y3	P3	Blue	Define shapes in P3
36 MMPoly1[b]	P1	Black	Defines shapes in P1
37 SacOx2_Cut [b]	X2C	Tan	Defines hole in X2
38 MMPoly2_Cut [b]	P2C	Red	Defines holes in P2
41 MMPoly3_Cut [b]	P3C	Blue	Defines holes in P3

a. Masks with "_Cut" in the name are dark-field masks (closed polygons define holes to be etched in film); others are light-field (Closed polygons define structures in film to be left after etch)

b. These "drawing-only" layers are XORed with their master layers to form the mask (i.e., P1C xor P1 = P1C, X2 xor X2C = X2, P2 xor P2C = P2, P3 xor P3C = P3). Shapes in drawing layers are only valid inside shapes in the corresponding master layer!

D.2 The SUMMiT Process

The following is a chronological description of the SUMMiT process. For ease in explanation, an example of fabricating a microengine will be discussed. Each of the following figures contain a plan view and cross-section of the microengine at various stages of the fabrication. The terms "poly" will be used interchangeably with "polycrystalline silicon", "oxide" with "silicon dioxide", and "nitride" with "silicon nitride". "Wet etching" generally refers to immersing the wafers in a bath of hydrofluoric acid (HF) for a certain length of time to etch away the sacrificial oxide. "Dry etching" generally refers to a process of applying reactive ion etching (RIE) to pattern a layer very selectively. Poly is generally etched using RIE and oxide is generally etched in a wet etching process. Generally, poly layers are patterned using an oxide mask while oxide layers are patterned using photoresist masks.

The SUMMiT process begins with a bare silicon wafer. A 0.63 µm layer of silicon dioxide (SiO2) is deposited on top of the bare wafer. This layer of oxide acts as an electrical insulator between the single-crystal silicon substrate and the first polycrystalline silicon layer (MMPoly0). A 0.8 µm thick layer of low-stress silicon nitride (SiNx) is deposited on top of the oxide layer. The nitride layer acts as an etch stop protecting the underlying oxide from wet etchants during processing. A 0.3 µm thick layer of doped polycrystalline silicon (Si) known as MMPoly0 is deposited on top of the nitride layer. MMPoly0 is not a structural layer, but it is usually patterned and is used as a mechanical

anchor, electrical ground, or electrical wiring layer. Following MMPoly0 deposition, the first sacrificial layer of oxide (SacOx1) is deposited. Tetraethylorthosilicate or TEOS is material used for all Sacrificial oxide layers. SacOx1 is 2 µm thick. Figure D.2 illustrates the state of the wafer after SacOx1 has been patterned and etched for dimples. Dimples will be formed from MMPoly1 (the next polysilicon deposition). The dimple etch is approximately a depth of 1.5 µm. Each dimple cut is approximately a 2 µm wide square with a depth of 1.5 µm.

Following the dimple etches, the SacOx1 is patterned for etches through the depth of the oxide to the MMPoly0 layer (Figure D.3). These SacOx1 etches are performed using reactive ion etching (very selective) and extend through the entire oxide layer, stopping at the interface between SacOx1 and the MMPoly0 layer. Polysilicon deposited over the SacOx1 layer will be anchored or bonded to MMPoly0 at the SacOx1 cuts, and will also act as an electrical connection between MMPoly0 and MMPoly1.

Figure D.2 Microengine insulating layers through Dimple1_Cut

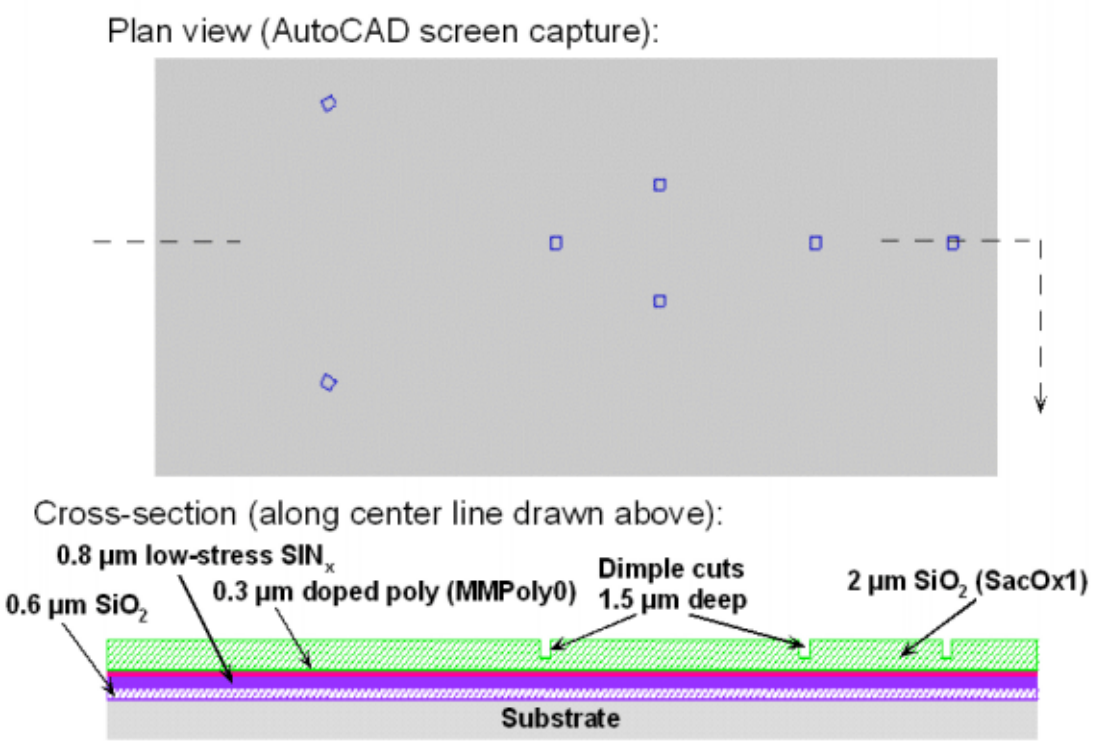
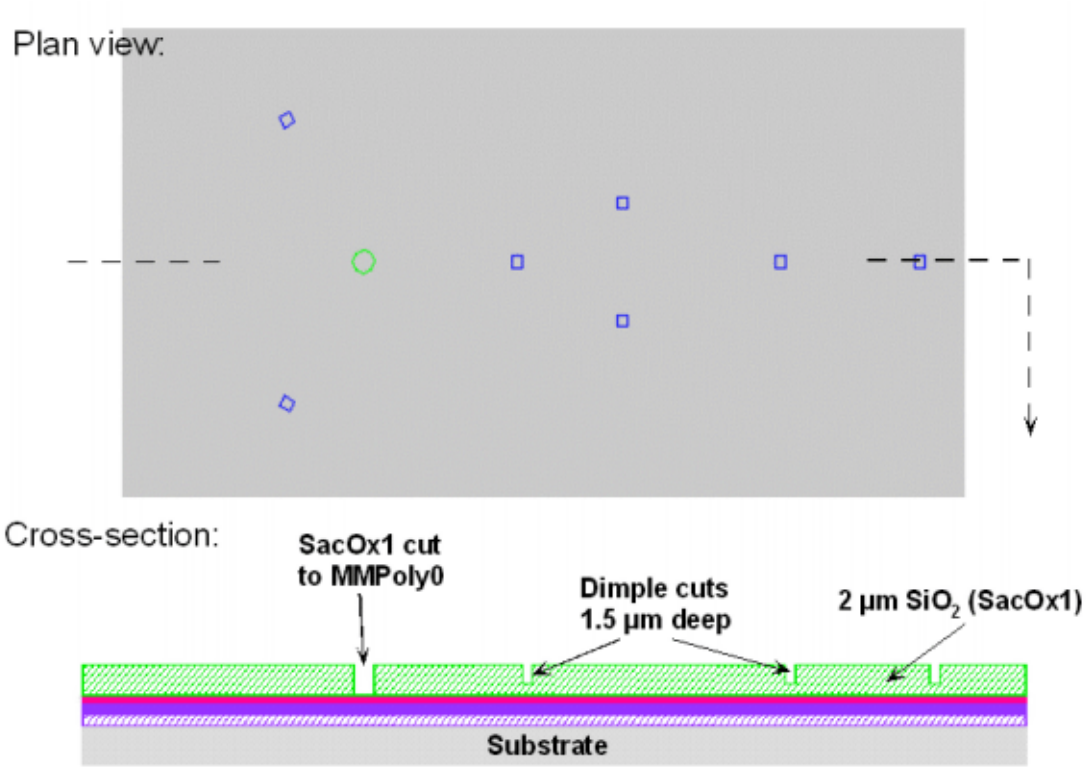


Figure D.3 Microengine SacOx1_Cut



Following SacOx1 cuts, a 1 µm thick layer of doped poly (MMPoly1) is deposited. The make-up of MMPoly1 is a 0.1 µm in-situ doped polysilicon sublayer plus a 0.05 µm undoped polysilicon sublayer plus a 0.85 µm undoped VTR poly sublayer which is then heated to migrate doping in the first sublayer to other sublayers in MMPoly1. Typically the polysilicon is doped with phosphine gas. Creating the microengine pin joint requires several steps. Following deposition, MMPoly1 is patterned and etched (using RIE) to open vias through the poly to SacOx1. The SacOx1 layer is then partially etched (using HF) to undercut MMPoly1 and create flanged geometry on the pin-joint and around the hub when subsequent layers of oxide and poly are added. Figure D.4 shows the formation of a pin-joint and pinion gear hub flange in the microengine.

Figure D.4 Microengine Pin_Joint_Cut

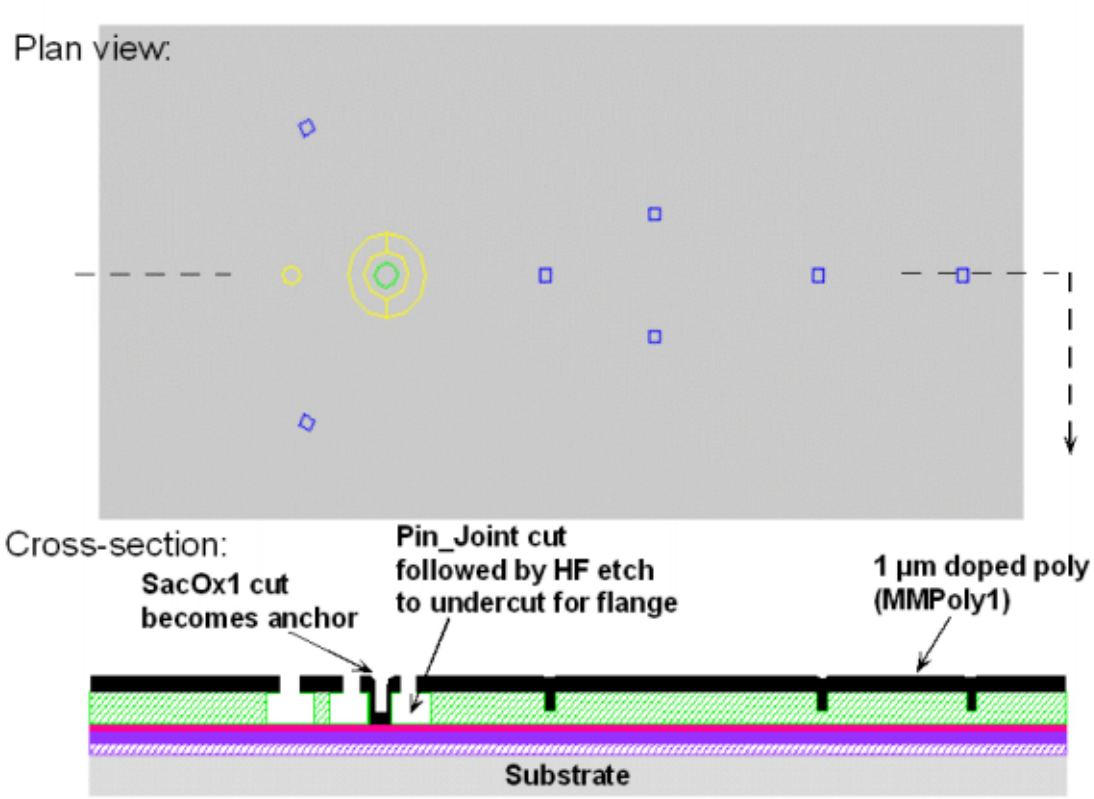
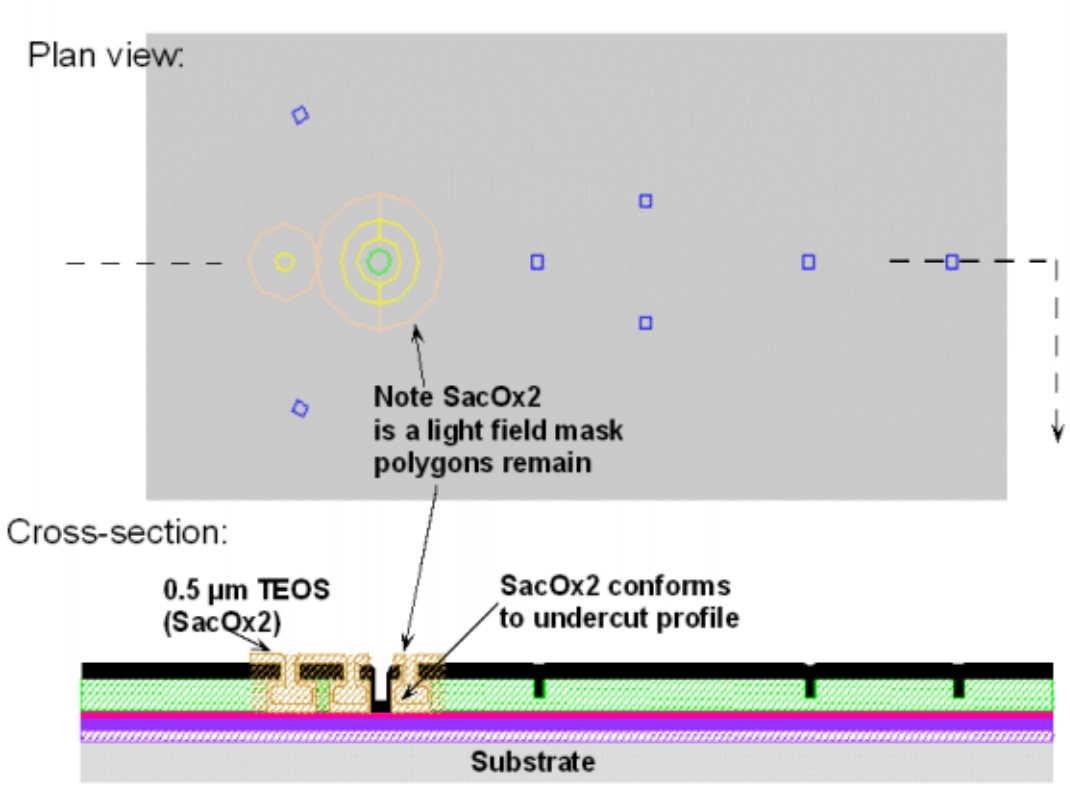


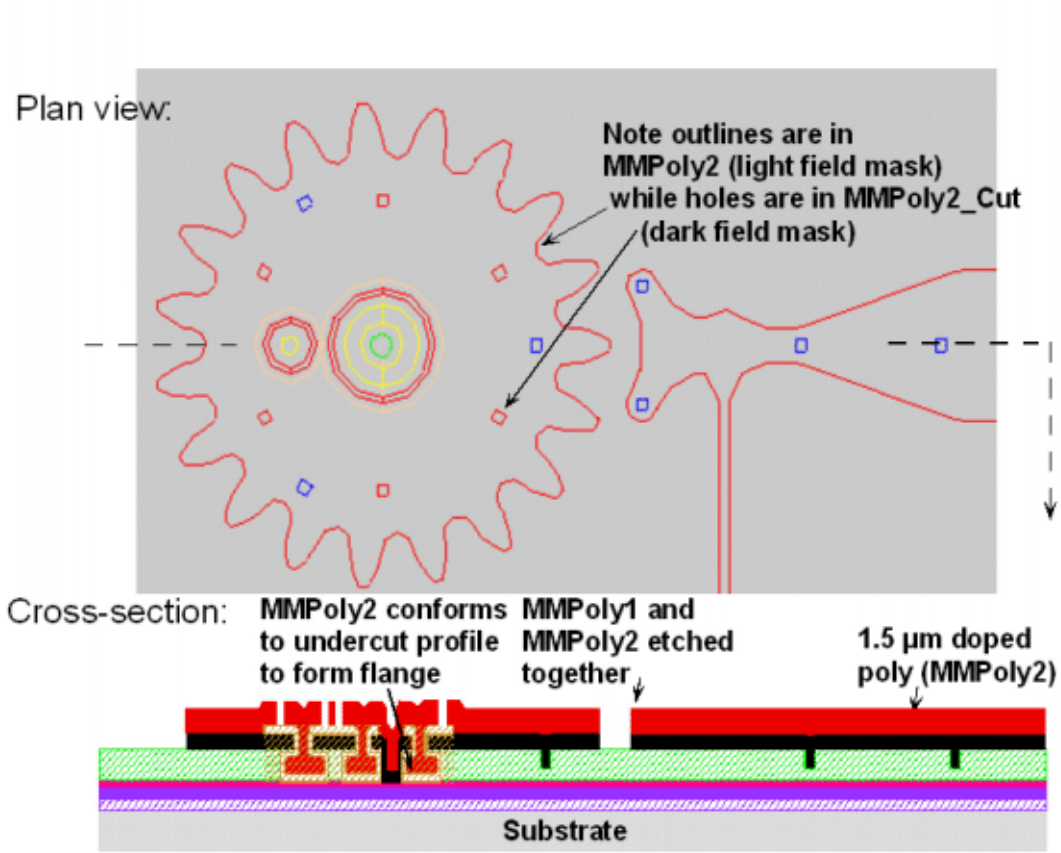
Figure D.5 depicts the deposition and patterning of 0.5 µm of TEOS oxide (SacOx2) on top of MMPoly1. The SacOx2 layer provides a conformal coating both on top of MMPoly1 and around the perimeter of the hub and pin-joint undercut regions below MMPoly1. Since SacOx2 is only 0.5 µm thick, it does not completely fill the undercut regions but leaves space for the next poly layer to form a flange.

Figure D.5 Microengine SacOx2



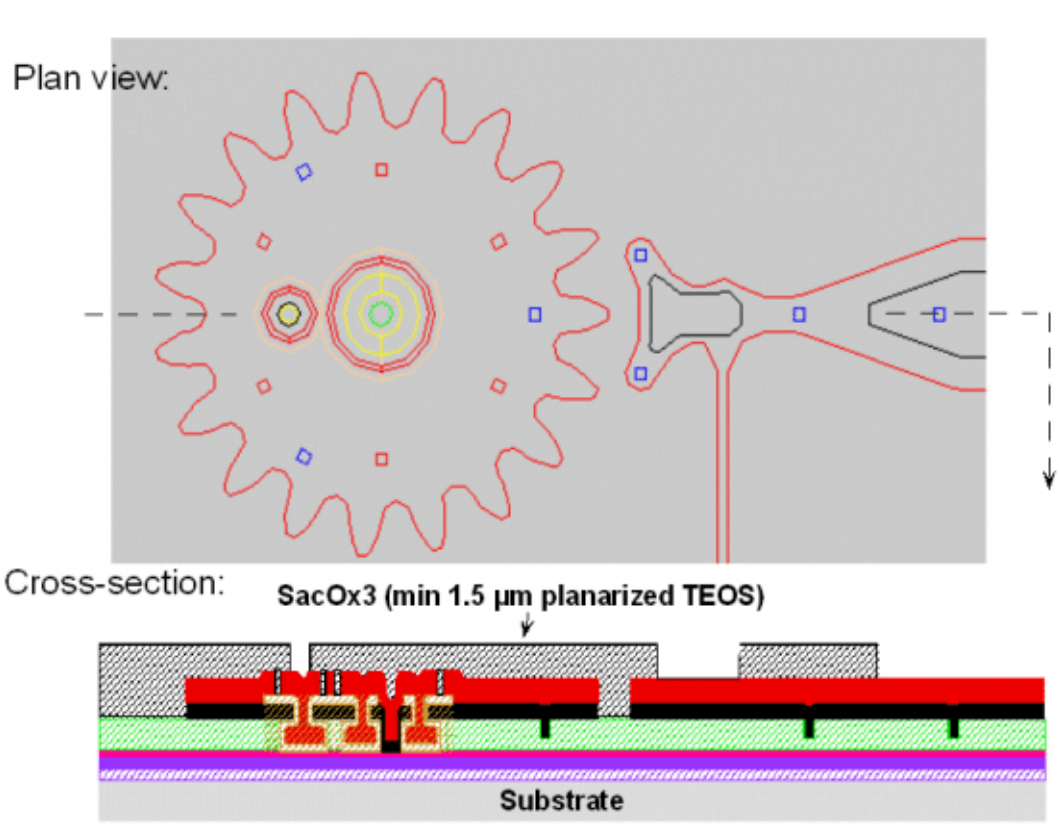
Following SacOx2 deposition, patterning, and etching. A 1.5 µm thick layer of doped polysilicon, MMPoly2 is deposited. The make-up of MMPoly2 is a 1.4 µm undoped VTR poly sublayer plus a 0.1 µm in-situ doped poly sublayer. MMPoly2 is capped with 0.3 µm of VTR TEOS and annealed for 3 hours at 1100°C which causes the dopant to migrate towards the center of both MMPoly1 and MMPoly2 layers. Doped areas etch faster than undoped areas so this improves the etching process as well as makes MMPoly1 and MMPoly2 better electrical conductors. MMPoly2 fills the undercut regions below MMPoly1 to form flanges for the pin-joint and hub. Following MMPoly2 deposition, a RIE etch is performed to etch composite layers of MMPoly1 and MMPoly2 (where they are laminated together to form a single layer approximately 2.5 µm thick). Figure D.6 shows the microengine after the MMPoly2 etch. It is important to note that the MMPoly2 mask is a single mask defined by combining two separate layers from the mask layout software (AutoCAD) by mathematically subtracting (XOR) regions defined in the MMPoly2_Cut mask from regions defined in the MMPoly2 mask.

Figure D.6 Microengine MMPoly2 XOR MMPoly2_Cut



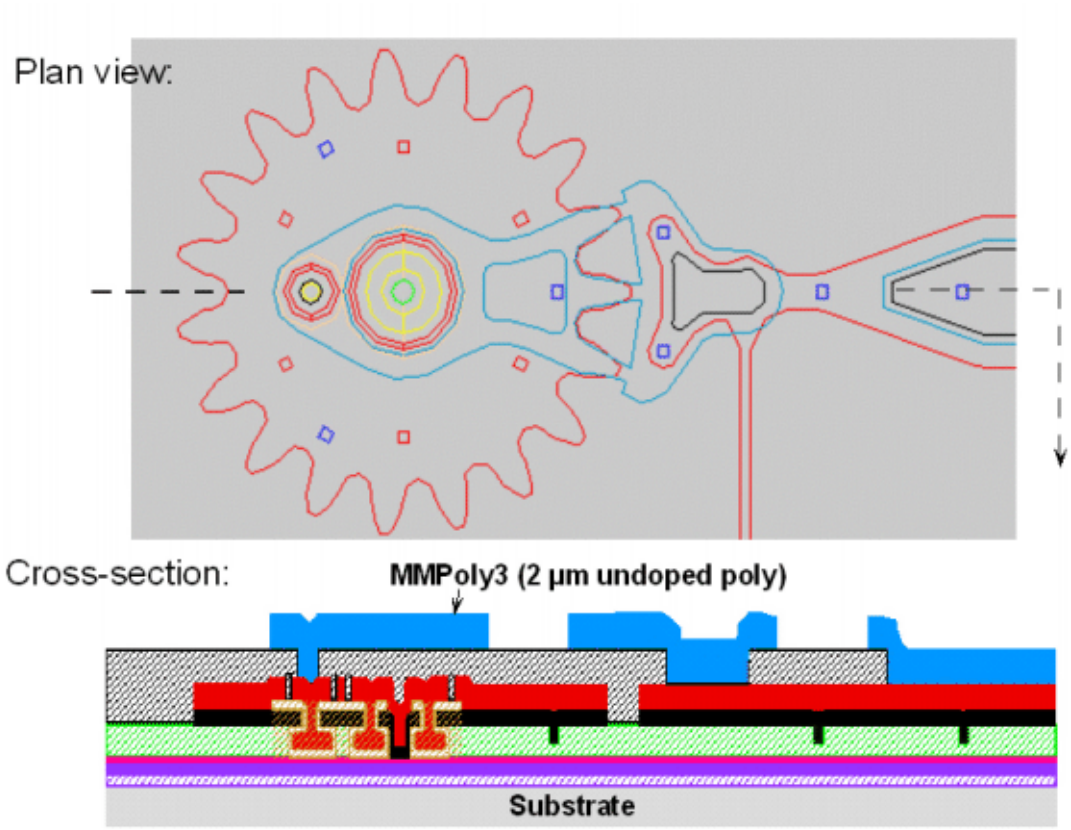
Following MMPoly2 etch, roughly 6 µm of VTR TEOS oxide (SacOx3) is deposited on the MMPoly2 layer. Chemical-mechanical polishing (CMP), is used to planarize the oxide to a thickness of about 2 µm. Following planarization, SacOx3 is patterned and etched (Figure D.7). Patterning and etching of SacOx3 is similar to SacOx1 in that both dimples and the geometry of the upper layer of poly are defined by etching SacOx3. Dimple cuts are etched completely through SacOx3 using RIE, then an additional 0.3 µm to 0.5 µm of oxide is deposited to provide a spacing layer between the bottom of the dimples (formed by deposition of MMPoly3) and the top of MMPoly2. Following the oxide backfill for the dimples, the cuts to SacOx3 are etched to create mechanical and electrical connections between MMPoly2 and MMPoly3.

Figure D.7 Microengine SacOx3_Cut



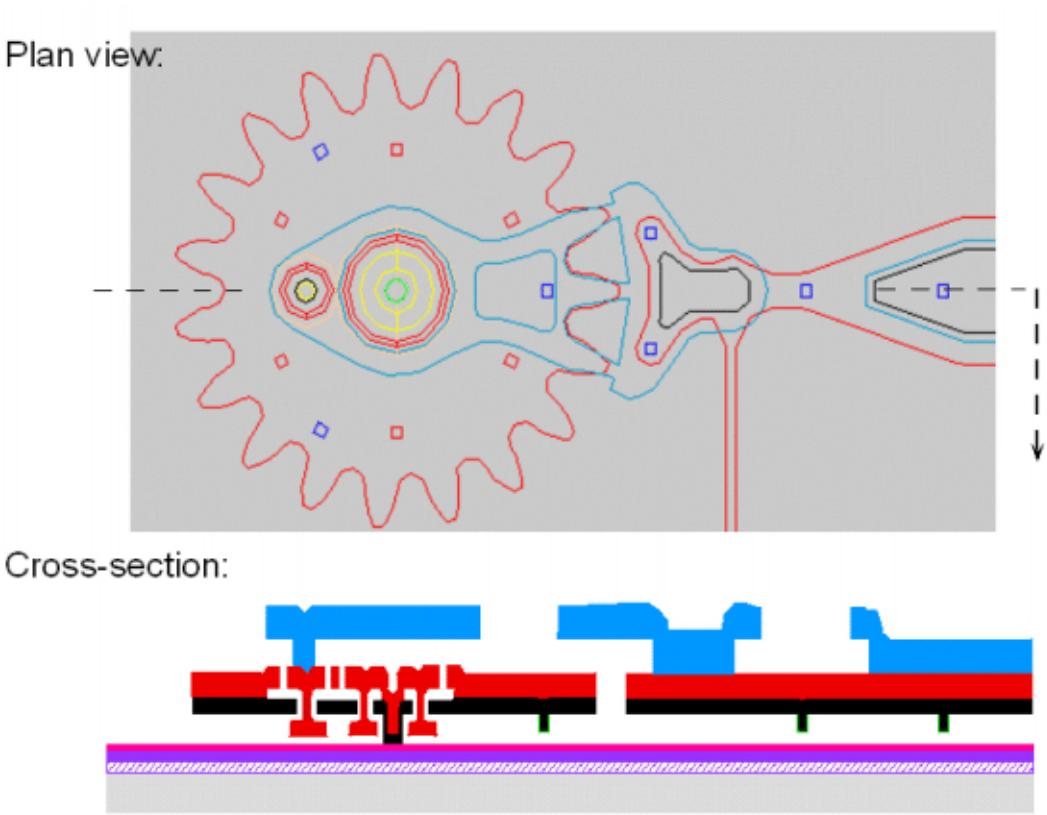
Following SacOx3 Etch, 2 µm thick layer of doped poly (MMPoly3) is deposited on the CMP planarized SacOx3 layer. This layer is capped with 0.5 µm of VTR TEOS and annealed for 3 hours at 1100°C. Figure D.8 shows MMPoly3 following deposition, anneal, pattern and etch.

Figure D.8 Microengine MMPoly3 XOR MMPoly3_Cut



After MMPoly3 has been patterned and etched, the microengine is released. The engine can be released by etching all the remaining, exposed oxide away with a 1:1 HF:HCL wet etch. Following the wet release etch, a drying process is employed using simple air evaporation, supercritical CO2 drying, or CO2 freeze sublimination. Figure D.9 depicts a released microengine.

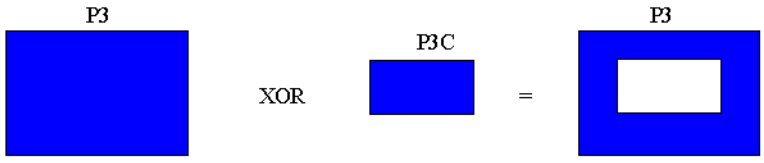
Figure D.9 Microengine released structure



D.3 A Side Note About SUMMiT Drawing Layers

Certain mask levels in SUMMiT have associated "drawing only" layers which are XORed with the master layer to form the final mask:

Master Layer	**Associated drawing layer**
MMPoly1_Cut (P1C)	MMPoly1 (P1)
SacOx2 (X2)	SacOx2_Cut (X2C)
MMPoly2 (P2)	MMPoly2_Cut (P2C)
MMPoly3 (P3)	MMPoly3_Cut (P3C)



Shapes in drawing-only layers (P1, X2C, P2C, and P3C) are only defined within shapes in their corresponding master layers (i.e. P1C, X2, P2, and P3, respectively).

In order to design with three independent poly layers (MMPoly1, MMPoly2, and MMPoly3) in SUMMiT, one can do the following:

1. Cover your entire module with the mask levels SacOx2 and MMPoly1_Cut.

2. Draw shapes in the MMPoly1 mask layer to define shapes in MMPoly1.
3. Draw shapes in SacOx2_Cut to define anchors between MMPoly1 and MMPoly2.
4. Take care not to nest the drawing levels (i.e., donít use a shape in MMPoly1_Cut to define a cut in a poly shape if you already have covered the entire module with MMPoly1_Cut).
5. Since MMPoly2 is not planarized, be careful of stringers!